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(NASA-CR-158370) SILICON ON CERAMIC PROCESS: SILICON SHEET GROWTH AND DEVICE DEVELOPMENT FOR THE LARGE-AREA SILICON SHEET AND CELL DEVELOPMENT TASKS OF THE LOW-COST SOLAR (Honeywell Corporate Material Sciences G3/31

N79-19175

Unclas
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DOE/JPL 954356-78/4
Distribution Category UC-63

SILICON ON CERAMIC PROCESS

Silicon Sheet Growth and Device Development for the Large-Area Silicon Sheet and Cell Development Tasks of the Low-Cost Solar Array Project

Quarterly Report No. 10

by

P. W. Chapman

J.D. Zook, J.D. Heaps, C. Pickering

B.L. Grung, B. Koepke, and S.B. Schuldt

Period Covered: 9/30/78-12/31/78

Published 31 January 1979

Honeywell Corporate Material Sciences Center
10701 Lyndale Ave. South
Bloomington, Minnesota 55420

The JPL Low-Cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, by agreement between NASA and DOE.

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SUMMARY

The objective of this research program is to investigate the technical and economic, feasibility of producing solar-cell-quality sheet silicon. We hope to do this by coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon from the melt.

Beginning the middle of February 1978, we expanded our program to include activities funded by the Task VI Cell Development Group of the Low-Cost Solar Array (LSA) program at the Jet Propulsion Laboratory. This work is directed toward the solution of unique cell processing/design problems encountered within the silicon-on-ceramic (SOC) material due to its intimate contact with the ceramic substrate.

The Task VI work is contained within this report and is labeled appropriately.

During the quarter, we demonstrated significant progress in several areas:

- The continuous (SCIM or Silicon Coating by an Inverted Meniscus) coater succeeded in producing small-area coatings exhibiting unidirectional solidification and substantial grain size.
- The experimental dip coater was put into operation and succeeded in producing thick, > 500 μm, dendritic layers at coating speeds of 0.2 to 0.3 cm/sec.
- We succeeded in developing a "standard" procedure for producing total-area SOC solar cells using slotted ceramic substrates. The best conversion efficiency performance to date is 9.6 percent (antireflective-coated AM1) on a 4-cm^2 total-area cell.

Other results and accomplishments during the quarter can be summarized as follows:

- A standardized process was defined enabling us to fabricate reproducible dip-coated layers for solar-cell processing by the Honeywell Solid State Electronics Center and other JPL contractors.
- A substrate dye-checking procedure was initiated following a suggestion by D. Wirth and J. Sibold of Coors Porcelain Co. This new procedure has increased our yield of silicon-coated slotted substrates.

- Observations were made which seemed to indicate that the liquid - solid interface tilts slightly away from the substrate contrary to what was originally thought.

- Remarkably consistent performance was achieved in Honeywell-fabricated SOC solar cells. The average total-area conversion efficiency on these cells was 8.3 (±0.8) percent [AR-coated, AM1].

- Three new mullite compositions were formulated by Coors for evaluation as slotted substrates.

- The fracture strengths of roll-compacted S1SI, J, K, and M Mod mullite substrates were measured.

- Several techniques for producing perforated mullite substrates were investigated by the Honeywell Ceramics Center. A technique for punching 1/8-inch-diameter holes in an MV-20 substrate produced a successful coating.

- Cooling shoes added to the experimental dip coater demonstrated that thick coatings can be achieved at higher pull speeds.

- Better thermal-gradient control at the solidification zone in the SCIM coater was obtained. This resulted in better quality small-area coatings. More-uniform temperature profiles at this critical point in the SCIM coater should produce more-uniform large-area coatings.

- Back Surface Field (BSF) investigations did not produce an effect in either single-crystal or SOC material.

- An analytical thermal analysis of the vertical SOC growth process was conducted. The model obtained suggests that the net lateral heat transfer in the neighborhood of the freezing front is into the ceramic as opposed to out from the free surface as originally thought.

INTRODUCTION

This research program began on 21 October 1975. Its purpose is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating inexpensive ceramic substrates with a thin layer of polycrystalline silicon. The coating methods to be developed are directed toward a minimum-cost process for producing solar cells with a terrestrial conversion efficiency of 12 percent or greater.

By applying a graphite coating to one face of a ceramic substrate, molten silicon can be caused to wet only that graphite-coated face and produce uniform thin layers of large-grain polycrystalline silicon; thus, only a minimal quantity of silicon is consumed. A dip-coating method for putting silicon on ceramic (SOC) has been shown to produce solar-cell-quality sheet silicon. This method and a continuous coating process also being investigated have excellent scale-up potential which offers an outstanding, cost-effective way to manufacture large-area solar cells. The dip-coating investigation has shown that, as the substrate is pulled from the molten silicon, crystallization continues to occur from previously grown silicon. Therefore, as the substrate length is increased (as would be the case in a scaled-up process), the expectancy for larger crystallites in-
c

iety of ceramic materials have been dip coated with silicon. The investigation has shown that mullite substrates containing an excess of SiO_2 best match the thermal expansion coefficient of silicon and hence produce the best SOC layers. With such substrates, smooth and uniform silicon layers 25 cm^2 in area have been achieved with single-crystal grains as large as 4 mm in width and several cm in length. Crystal length is limited by the length of the substrate. The thickness of the coating and the size of the crystalline grains are controlled by the temperature of the melt and the rate at which the substrate is withdrawn from the melt.

The solar-cell potential of this SOC sheet silicon is promising. To date, solar cells with areas from 1 to 10 cm^2 have been fabricated from material with an as-grown surface. Conversion efficiencies greater than 9 percent antireflection (AR) coated have been achieved without optimizing cell processing techniques. Such cells typically have open-circuit voltages and short-circuit current densities of 0.54 V and 23 mA/cm^2, respectively.

The SOC solar cell is unique in that its total area is limited only by device design considerations. Because it is on an insulating substrate, special consideration must be given to electrical contact to the base region. One method which offers considerable

promise is to place small slots in the substrate perpendicular to the crystalline growth direction and contact the base region by metallizing the silicon that is exposed through the slots on the back side of the substrate. Smooth, continuous coatings have been obtained on substrates which were slotted in the green state prior to high-temperature firing. The best slotted-cell results indicate a 9.6 percent conversion efficiency (AR-coated) on a 4-cm^2 (total area) cell. This cell was not optimized for device performance.

Development efforts are continuing in such areas as improvement in growth rate, reduction of progressive melt contamination, and optimization of electrical contacts to the base layer of the cell. The investigation has shown that mullite substrates, to a limited extent, dissolve in molten silicon. The impurities from the substrate are believed to adversely affect solar-cell conversion efficiency. A method for reducing substrate dissolution is to reduce the contact area the substrate makes with the silicon melt. Therefore, a silicon coating facility, referred to as SCIM or Silicon Coating by an Inverted Meniscus, has been constructed which is designed to coat large (10-cm x 100-cm) substrates in a continuous manner. It is expected that this facility will not only improve the growth rate, but also minimize the silicon melt contact with the substrate. This should reduce the rate at which the melt becomes contaminated. The facility will also permit a study of possible continued grain growth by accommodating the use of longer substrates. It should also reveal problems that are likely to be encountered in a scale-up process. This machine has succeeded in demonstrating coatings exhibiting unidirectional solidification (desirable and occurring in dip coating) but has yet to achieve continuous coating of a 100-cm-long substrate.

TECHNICAL DISCUSSION

SUBSTRATE DEVELOPMENT AND CHARACTERIZATION
(B. Koepke and K. Jatavallabhula)

During the quarter, substrate activity was concentrated principally in the following three areas: 1) the evaluation of slotted substrates made from two new compositions (M and N modifications) manufactured by Coors Porcelain Co.; 2) characterization of the mechanical properties of these compositions at Honeywell's Corporate Material Sciences Center (CMSC), and 3) investigation of different techniques of perforating substrates carried out by the Honeywell Ceramics Center (HCC). These three areas are discussed below.

Substrate Evaluation

Three new compositions were produced by Coors Porcelain Co. for substrate evaluation. These compositions, designated L, M, and N modifications, are listed in Table 1.[1]

Table 1. Composition of Various Mullite Bodies

Code	Material	Approximate Percent Oxide Composition									Ratio
		Al_2O_3	SiO_2	Fe_2O_3	CaO	MgO	K_2O	Na_2O	TiO_2	B_2O_2	Al_2O_3/SiO_2
1A	Std. S1SI Coors composition	57.6	38.9	0.62	0.13	0.25	0.92	0.25	1.12	0.00	1.48
K	184 HRM 72.5% S1SI 27.5% SiO_2	41.4	56.2	0.45	0.14	0.18	0.66	0.18	0.81	0.00	0.74
L	71.43% S1SI 28.57% SiO_2	40.7	56.9	0.45	0.14	0.18	0.66	0.18	0.79	0.00	0.715
M	69% S1SI 31% SiO_2	39.2	58.4	0.43	0.14	0.17	0.64	0.17	0.77	0.00	0.67
N	Calcined clay plus SiO_2 (K-747 + K-135)	41.0	56.5	0.89	0.02	0.04	0.02	0.03	1.56	0.00	0.73

Also included in Table 1 are the standard S1SI composition and the most recent batch of K Mod material. The thermal expansion coefficients (RT to 800°C) for the K, L, M, and N modifications were 3.98, 3.78, 4.31, and 3.64 x 10^{-6} $°C^{-1}$, respectively. The high

value for the M material was due to a higher than anticipated Al_2O_3/SiO_2 ratio as detected by chemical analysis of the fired material.[2] The compositions listed in Table 1 are based on initial batch compositions rather than an analysis of fired bodies. The higher expansion of the M Mod material is corroborated by our observation that this material had a greater tendency to fracture during dip coating. The L Mod material had not been delivered to CMSC as of the end of the quarter and thus was not evaluated.

Substrate Mechanical Properties

The fracture strengths of roll-compacted S1SI, J, K, and M Mod substrates were measured at room temperature in four-point bending and are listed in Table 2. The samples were nominally 0.04-inch thick and 0.12-inch wide and were tested over an inner and outer span of 0.5 and 1.25 inches, respectively. The crosshead speed was 0.01 inch/minute.

Table 2. Fracture Strengths of Roll-Compacted Substrates

Code	Material	Strength (kpsi)
A	S1SI (155 RCM)	17.6 ± 2.7
J	J Mod (183 RCM)	11.1 ± 1.5
K	K Mod (184 RCM)	14.0 ± 1.6
M	M Mod (218 RCM)	13.1 ± 2.8

The strength of the roll-compacted S1SI is slightly less than the cold-pressed and sintered material (21.7 kpsi as reported in Annual Report No. 3). Increasing the silica content appears to decrease the strength. This is expected because the higher SiO_2 materials contain less mullite. The decrease is apparently not systematically related to the amount of SiO_2 in the material.

Substrate Perforation Techniques

In work carried out at the Honeywell Ceramics Center, W. Harrison and G. Hendrickson have been examining different means to produce perforated mullite substrates. In one attempt, a slurry mix of pure alumina and pure silica was cast on a surface from which metal pins protruded in order to perforate the substrate during initial drying. Due to shrinkage, the cast bodies fractured during drying. In a second attempt, the slurry was cast around pins protruding from a sheet of silicone rubber. The body was removed from the pins and dried; it remained intact but the holes "healed" shut. In a third attempt, extrudable McDanel MV-20 mullite was rolled and then 1/8-inch-diameter holes were

punched in the sheet on 1/4-inch centers by hand. This technique was successful and a number of perforated substrates were delivered to the Corporate Material Sciences Center for evaluation.

To date, one punched MV-20 substrate has been dip coated with silicon. The following points were noted:

- The substrate coated uniformly but the coating contained depressions corresponding to where the coating bridged a hole.
- The substrate did not crack.
- Many of the holes were filled with silicon.

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Photographs of the coated MV-20 substrate are shown in Figure 1. The irregular nature of the surface is shown in the left-hand photograph. The back side of the substrate is shown in the right-hand photograph. Some holes that appear filled with silicon are indicated by arrows. Note that the holes appear filled but in all cases are only coated on the top and bottom with a thin layer of silicon. The mechanism for this behavior is uncertain and is under study. This phenomenon is observed with holes but not with slots. The difference may be due to dynamic effects occurring when the meniscus passes a hole or slot. When it passes a slot, it breaks on the back side but, in some cases, does not break over a hole.

(a) (b)

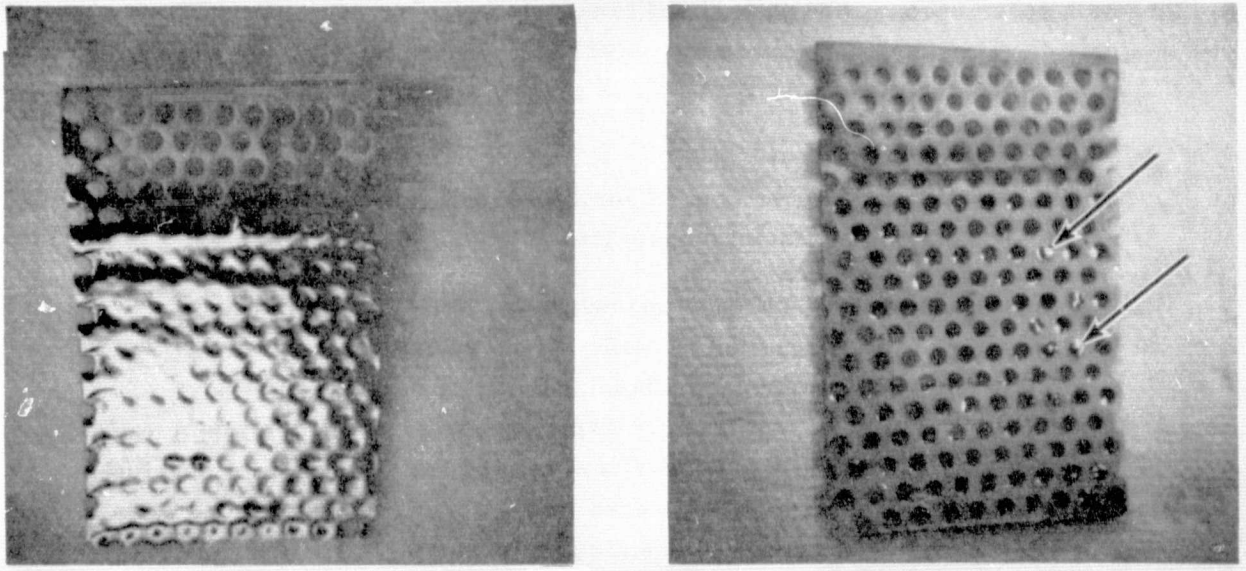

Figure 1. Photographs Showing (a) the Front and (b) the Back Side of a McDanel MV-20 Perforated Mullite Substrate that was Dip Coated with Silicon. The substrate measures 1.75 x 1.75 x 0.070 inches. The holes are approximately 3/32-inch in diameter and are approximately 3/16-inch apart. Arrows indicate where the holes appeared filled with silicon.

SHEET SILICON GROWTH (J. D. Zook, J. D. Heaps, L. D. Nelson, D. J. Sauve, R. Hegel, and H. Burke)

Dip-Coating Production

During the quarter, emphasis was placed on increasing the production output of dip-coated SOC material. There were two basic reasons for this: 1) to supply the Honeywell Solid State Electronics Center (SSEC) with material for processing into solar cells, and 2) to supply JPL with substrates to be processed by other contractors -- namely, OCLI and Spectrolab.

A standard procedure was defined, and a production schedule was developed to supply the demand with the original dip-coating system. Due to a number of operational problems, we were not able to meet that schedule with the single system, so the experimental dip-coating system was also used for production.

The standard procedure is described as follows:

1) All carbon parts used in the dip-coating system are purified and certified to contain less than 10 ppm of Ti, V, and Fe. Unfortunately, we were not able to maintain all parts to this specification with respect to Fe, but the parts were checked by the Honeywell Chemistry Laboratory by emission spectroscopy, and were found to contain less than 100 ppm Fe in all cases. This is in contrast to the uncertified carbon parts we previously used which contained 1500 ppm Fe, as well as significant amounts of Ti and V.

2) The substrates are Coors "type K" mullite-based ceramic with a demonstrated expansion coefficient closely matching that of Si.

3) The substrates are dye-checked and baked at 1000°C. This procedure was initiated at the suggestion of ceramics consultants from Coors Porcelain (Dave Wirth and Jack Sibold). During a recent visit, they carefully observed the growth in the experimental dip-coating system (which has excellent viewing access) and noticed that cracks were developing in the ceramic when it was lowered into the melt. These cracks were in all likelihood present in the ceramic before dipping. They suggested the dye-checking procedure which reveals cracks in the substrates, followed by firing at 1000°C in air to burn off the dye and any residual hydrocarbons due to handling. After firing, care is taken not to touch the substrates except with plastic gloves. Results in the experimental dip coater indicate that the new procedure has considerably reduced the substrate cracking.

4) Hand-rubbed carbon coatings are applied to the sample using spectrographic carbon. We realize that the hand-rubbed carbon is not ideal because the coverage is not as uniform as with the colloidal graphite paint. However, at present, hand-rubbed carbon is the only method that assures that carbon does not enter the slots. If carbon enters the slots, the silicon wets the slots and does not get forced out during solidification. The latent heat released during solidification upsets the crystal growth conditions, and crystallinity is disturbed.

5) Argon is introduced into the system just above the melt surface in the vicinity of the growing crystal to sweep away the SiO particles generated in the melt.

6) In addition to the foregoing, the procedure calls for the following:

   a) 600-gram charge
   b) 600×10^{16} atoms boron dopant
   c) 30-minute prebake of substrate just prior to dipping
   d) 1.6 cc/minute argon flow rate
   e) 3-minute preheat at 1/8-inch above melt
   f) 20-second soak time in melt
   g) 0.06 cm/sec pull rate
   h) 2-minute stabilization just after meniscus breaks
   i) 0.06 cm/sec initial withdrawal for 2 inches

With the above procedure, the production yield improved during the quarter. The velocity of 0.06 cm/sec gives layers 200 to 250 μm thick. The remaining production problems were associated with the power supply and temperature controllers, availability of substrates, and changes in operator personnel.

There is one yield-limiting factor which is not understood. During some of the runs, some of the samples developed dendrites in the center region of the sample. The dendrites can be eliminated by raising the melt temperature, but this results in a decrease in layer thickness, and the increased possibility of the silicon layer not bridging the slots. The appearance of the dendrites in the middle of a layer suggests some change in the thermal conditions during growth, but the cause of such a change is not apparent.

During the quarter, type M substrates from Coors were also evaluated for dip coating. These substrates have a higher glass content than the type K substrates. They have

suffered significant breakage problems during dipping and appear to be too soft at the melting point of silicon. Further evaluation will be done when we have caught up with the production schedule.

Experimental Dip Coater

During the quarter, a new dip-coating facility was put in operation at CMSC. A photograph of the dip coater is shown in Figure 2. The unit is basically the same as the existing dip coater but is larger and affords greater accessibility to the molten silicon by the operator. The other dip coater is seen in the background of Figure 2. The power supply is situated between and is shared by both units. There are four access ports in the central section of the new dipper. Two are inclined at 11 degrees to the melt surface and two are at 30 degrees. The melt surface is typically maintained level with the parting line between the lower and middle chambers, and all access ports focus on the center of the crucible at this level. There are four access ports in the top of the chamber inclined at about 60 degrees to the melt surface. The crucible supports and pulling mechanisms in the new dipper are identical with the other unit but the heater is different. In the new unit we have installed a graphite resistance heater with a picket fence design rather than the thin-wall heater used in the other unit.

The new heater assembly is shown in Figure 3. The glass tube on the right side of the heater is used to blow argon gas over the melt surface during some runs to minimize SiO formation on the silicon coating. The picket fence heater is believed to be less susceptible to damage and provide more-uniform heating than the thin-wall heater used in the other system.

In 1979, the new dip-coating facility will be used mainly to determine how the throughput of the SOC process can be optimized. The major goal will be to define conditions under which reasonably thick (i.e., 100 μm) silicon coatings can be grown at relatively high rates (i.e., 0.15 to 0.3 cm/sec). With the dip-coating geometry used to date, the velocity - thickness relation follows that discussed in Annual Report No. 3, namely v^2t = constant. This behavior has also been found in the new dipper. Figure 4 shows coating thickness plotted as a function of pull rate for a series of coatings made on unslotted Coors K Mod substrates in the new dipper. The dotted lines in the figure show the spread in all the data taken on the other dipper and published as Figure 10 in Annual Report No. 3. The data taken with the new dipper follow the relation $v^{2.3}t$ = constant. The goal of the program to increase the throughput is also shown in the figure.

The data plotted in Figure 4 represent the upper limit in coating thickness expected with the experimental arrangement currently in use (i.e., simply withdrawing a substrate from a crucible of molten silicon). In this case the radiative and convective cooling of the silicon coating is dictated by the melt temperature, the growth velocity, and the thermal conditions of the environment (e.g., the temperature of the walls of the chamber).

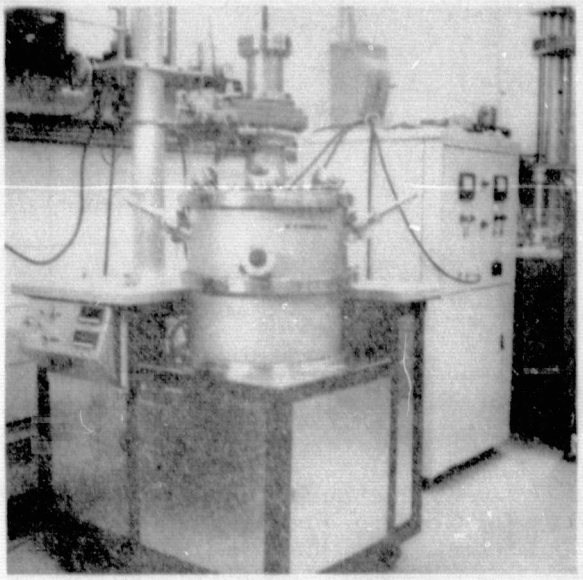

Figure 2. Photograph of New Dip-Coating Facility

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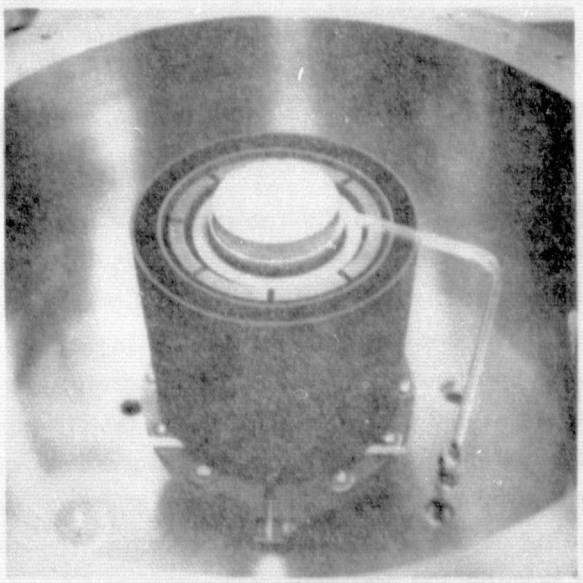

Figure 3. Photograph of Heater and Crucible in New Dip Coater

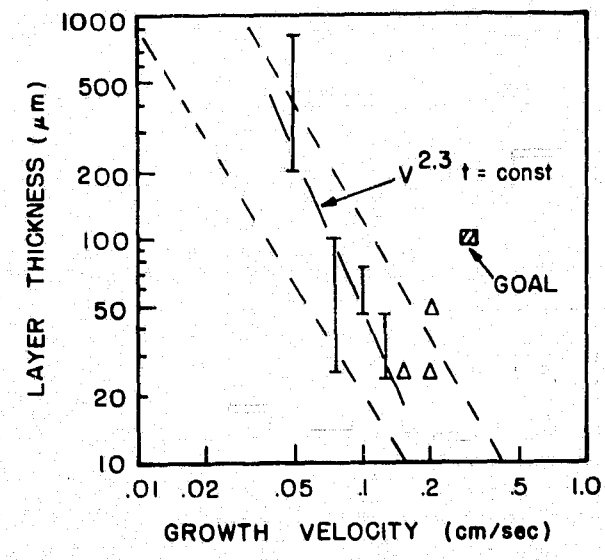

Figure 4. SOC Layer Thickness Plotted as a Function of Pull Rate for Coatings Produced on Unslotted Coors K Mod Substrates in the New Dip-Coating Facility. The triangles represent data taken with external cooling employed.

If thicker coatings are to be produced at increased pull rates, external cooling will have to be used. Experiments with external cooling have been started. Cooling in the vicinity of the liquid - solid interface is being provided by the two cooling shoes shown in Figure 5. The shoes are mounted on rods that protrude from two of the 30-degree access ports as shown in Figure 2. The shoes are positioned so that both sides of the substrate can be cooled during coating. The cooling shoes are machined from nickel billets and are cooled by water flowing through the rods and into passages drilled in the shoes. One of the shoes has gas jets drilled in it to allow a stream of gas to be directed at the substrate during coating. The gas also enters the shoe through the support rod.

Several preliminary runs were made with the cooling shoes in place. These data are plotted in Figure 4 as triangles. Substrates were pulled at 0.15 and 0.2 cm/sec with the water-cooled cooling shoes positioned 6 mm from both sides of the substrate and about 6 mm above the melt. The cooling shoe on the coating side contained gas jets and allowed a stream of argon to be directed on the silicon coating. Figure 6 is a photograph of an SOC coating made at 0.2 cm/sec under these conditions. Most of the silicon had solidified dendritically, indicating the melt temperature was too low for the conditions used. The upper data point on Figure 4 at 0.2 cm/sec was measured on the smooth portion of the coating existing on the lower right-hand side of the substrate. These are preliminary results and it is expected that improvements will be made in the coating quality as the growth conditions are optimized.

A notable point concerning these early runs with external cooling is that cracking was not observed. This important observation indicates that afterheaters may not be necessary even at high pulling rates. This appears to be a major advantage of supported growth.

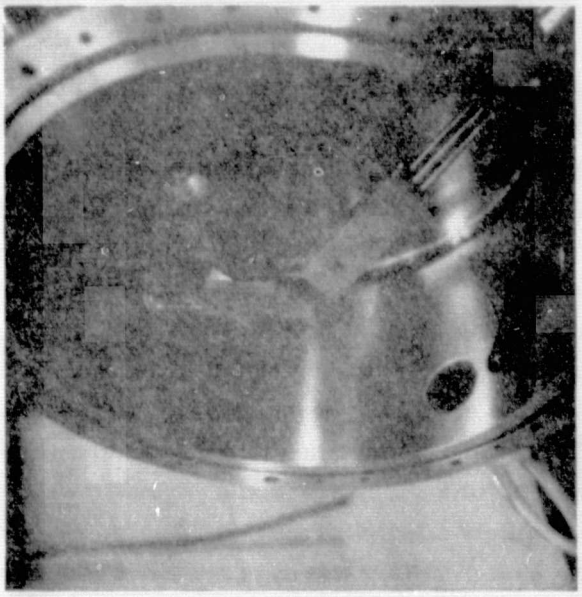

Figure 5. Photograph of Upper Chamber of New Dipper Showing Cooling Shoes

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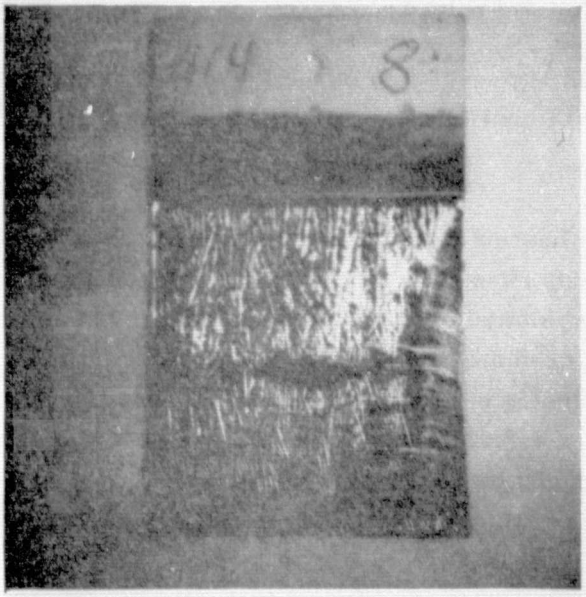

Figure 6. Photograph of Substrate Dip Coated with Silicon at a Pull Rate of 0.2 cm/sec with Cooling Shoes in Place Near Front and Back Sides of Substrate. With the exception of the lower right-hand side of the sample, the coating is dendritic.

Continuous Coating Process

A good part of this reporting period was spent making SCIM coating operational runs. After performing a number of these runs with various heating-element temperature combinations, it became apparent that the trough heating design shown in Figure 7 was not likely to allow the coating on the substrate to solidify at a distance less than 1 inch downstream of the trough. When the liquid - solid interface occurs this far downstream, there is a tendency for molten silicon to be drawn from the trough as the substrate skims over it. This is particularly true at slower (< 0.1 cm/sec) coating speeds where, as with dip coating, more silicon is pulled from the melt to accommodate a subsequently thicker layer. To correct this condition, a new type trough-heater assembly was installed in the coater. The original trough heater also served as a final substrate heater. This was needed to ensure that the substrate would be sufficiently high in temperature before it passed over the molten-silicon meniscus. The new heater assembly also serves this function. The heater is fabricated in such a way that the graphite trough holder itself is an active resistive element of the assembly (see Figure 8). The rectangular legs of this heating assembly fill the final substrate heating requirement. The power density of each leg is graduated in such a way that the substrate temperature never exceeds the melting point of silicon, as shown in Figure 9. Contrary to the original approach, the heating zone now terminates abruptly at the downstream edge of the trough.

Operational runs following this modification revealed that under favorable conditions the solidification interface can be made to occur within 1 cm of the trough. This dimension varied with respect to the temperatures of the trough and upper substrate heaters, as well as with the quantity of cooling gas that can be directed on the silicon-coated face of the substrate.

Runs made with this new heating configuration produced small-area (~ 20 cm^2) coatings. As experienced in previous runs, the silicon meniscus was gradually drawn from the trough as the substrate skimmed over it. Since our first attempt to SCIM coat, we have observed that the extent to which molten silicon is drawn from the trough varies with the velocity of the moving substrate. At faster velocities (> 0.1 cm/sec), the substrate travels a greater distance before this withdrawal takes place than is possible at slower speeds. Since coating thickness is a function of substrate speed, this overflow problem makes it difficult to achieve thicker, well-developed crystalline layers of any significant length.

The upper substrate heater could also be a heat source which prevents the solidification front from occurring immediately downstream of the trough (see Figure 9). Note that this heater extends beyond the trough. In a continuing effort to steepen the temperature gradient in this zone, the length of this heater was reduced as shown in Figure 10.

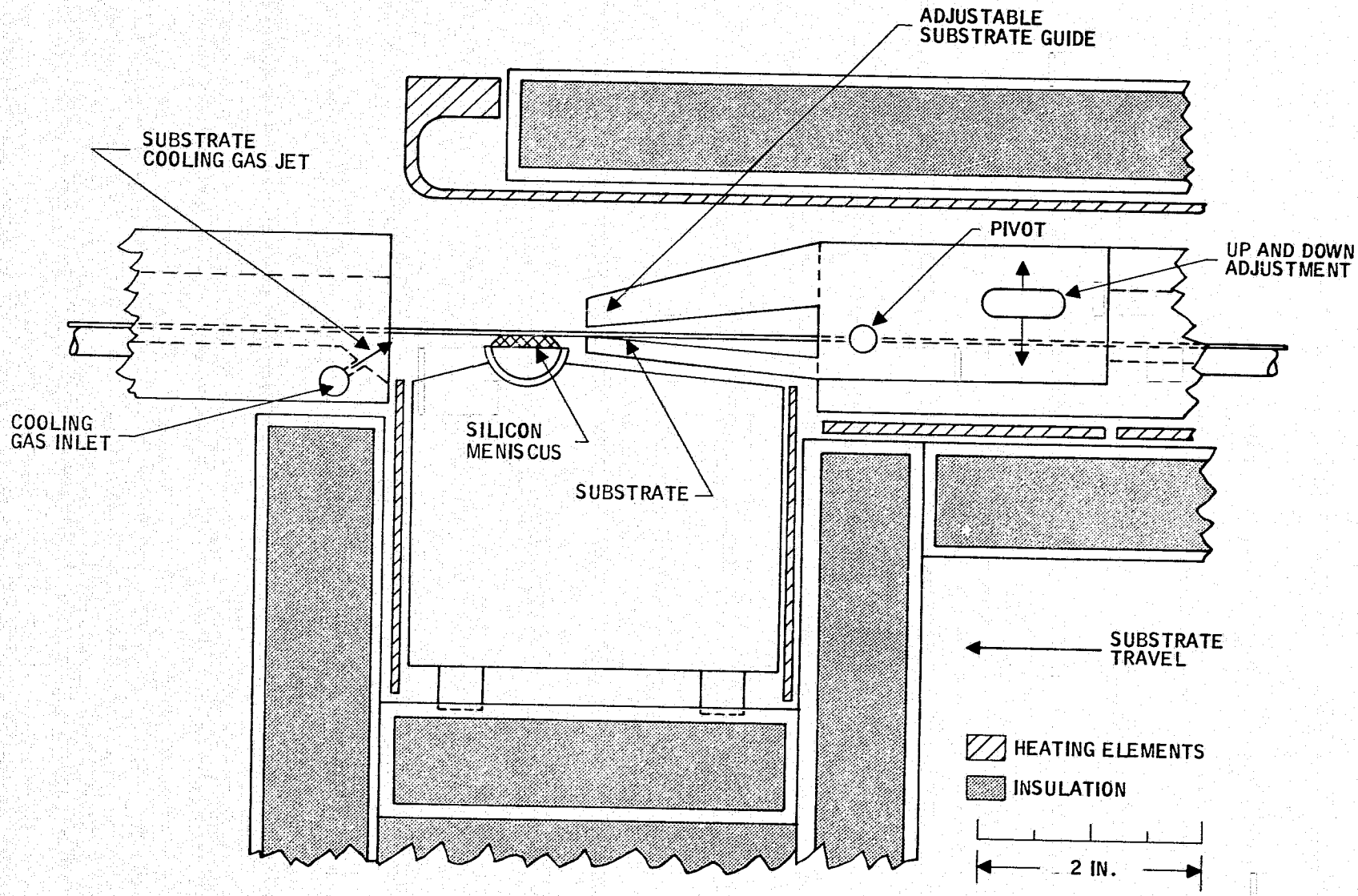

Figure 7. Growth Chamber Cross Section Showing Adjustable Substrate Guide and Substrate Cooling Gas Ports

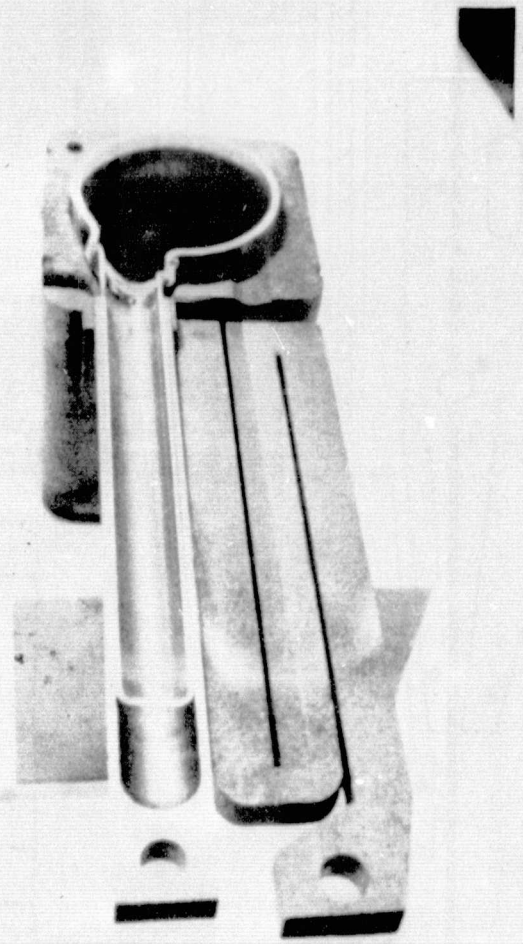

Figure 8. Photograph of New Trough/Substrate Heater (Also Showing Quartz Crucible/Trough Piece)

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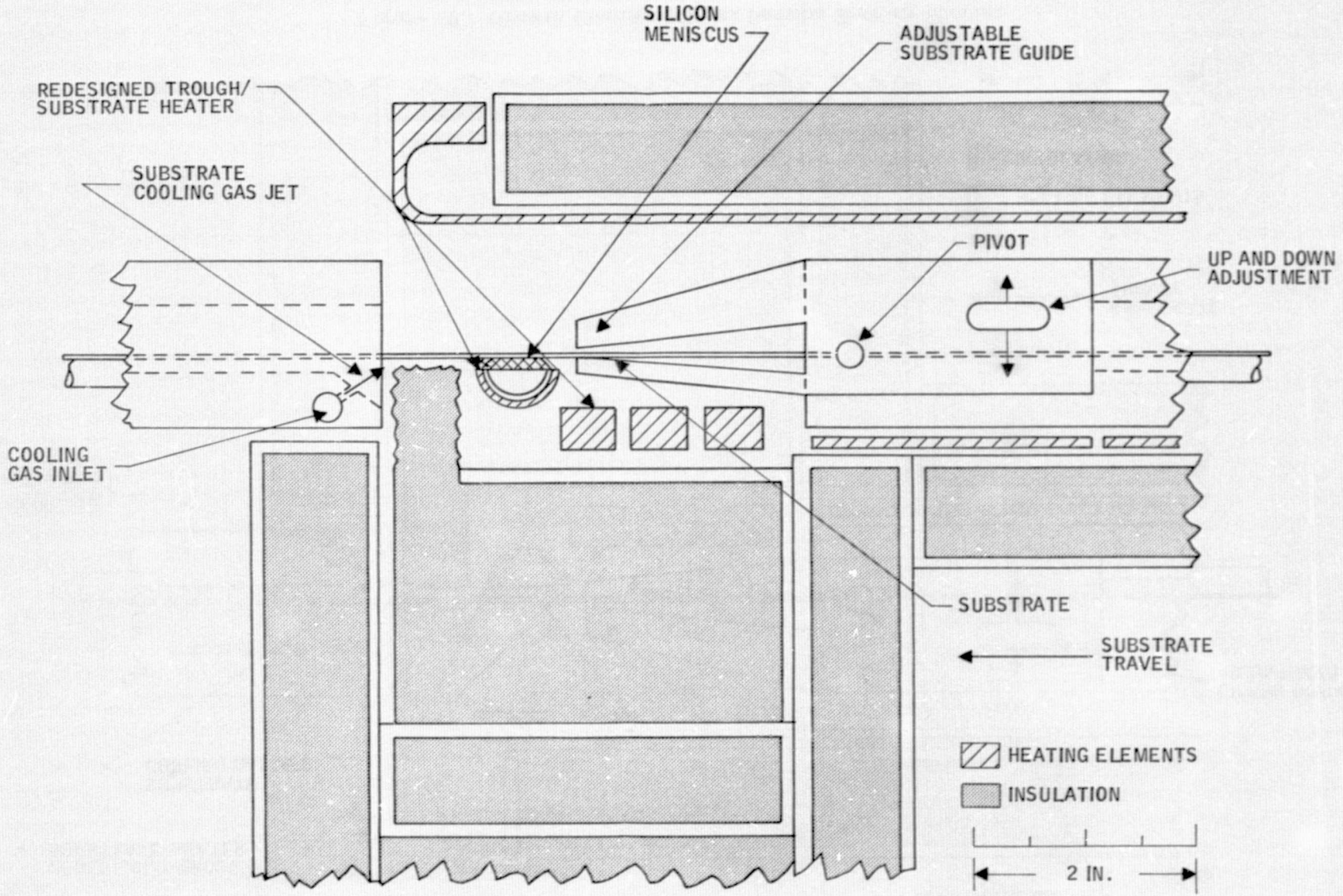

Figure 9. Growth Chamber Cross Section Showing Newly Designed Trough/Substrate Heater

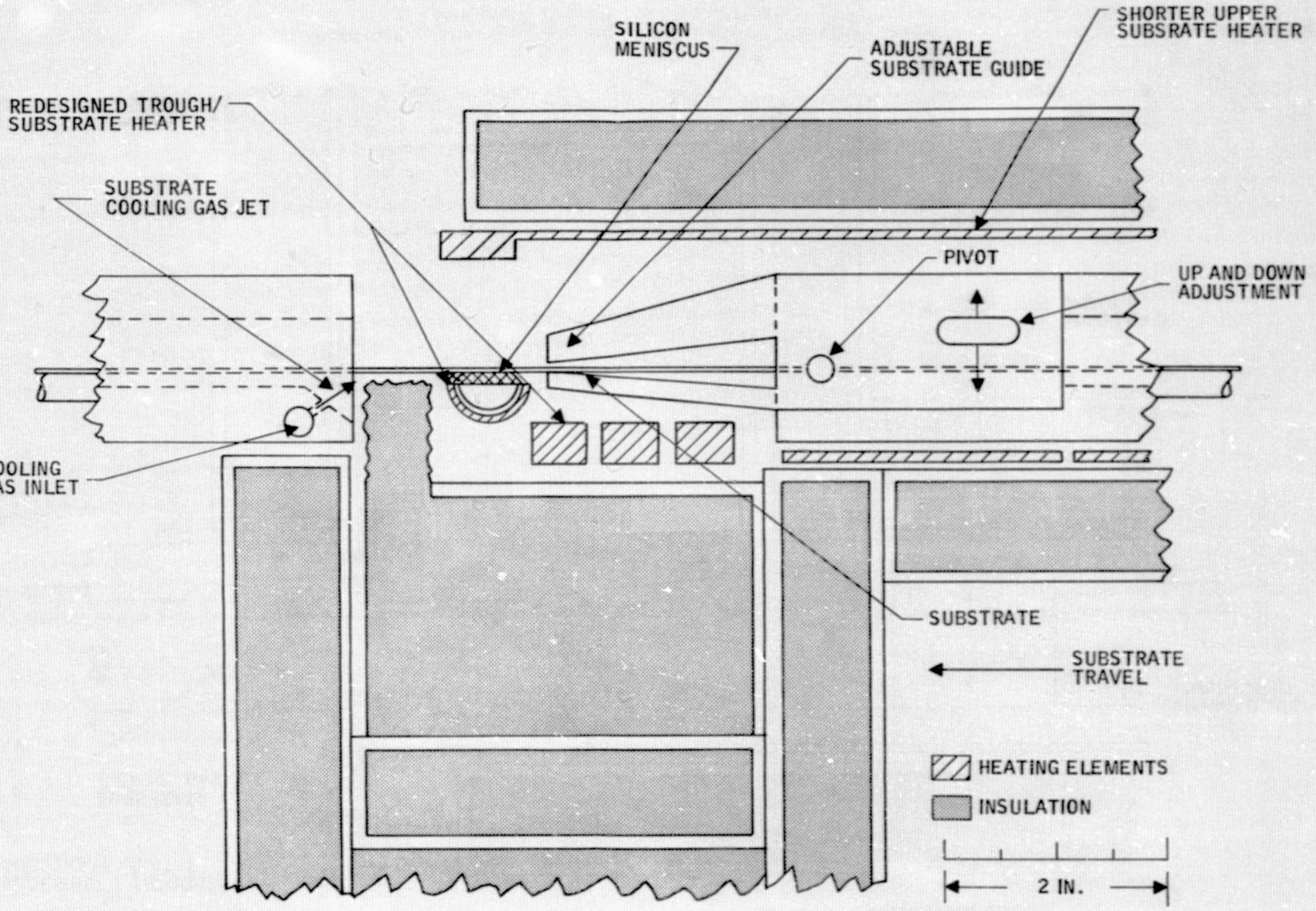

Figure 10. Growth Chamber Cross Section Showing Shorter Upper Substrate Heater

With this shorter heater, the interface, if desired, can now be shifted until soldification occurs at the edge of the trough. This is the dip-coating equivalent of having the surface of the melt freeze around the substrate as it is being withdrawn from the melt. The temperature of this shorter heater is now a critical coating parameter. If too hot, solidification, as usual, occurs too far downstream. If insufficiently hot, the substrate will freeze to the melt. Using the latter of these two thermal conditions, however, promising layers have been achieved by raising the meniscus height and, consequently, the substrate level as it passes over the meniscus. Apparently the additional heat of fusion contained in this larger volume of silicon prevents the freeze-up which normally occurs with a lower meniscus. Unfortunately, temperature nonuniformity along the trough prevents the solidification front from occurring in a single plane which runs parallel to the trough. The portions of this front which are downstream from the trough continue to allow molten silicon to be pulled from the trough. This temperature nonuniformity was introduced by the new trough heater design and measures must be taken to correct this problem.

Small-area (10 to 15 cm^2) coatings have nevertheless been made under these nonuniform thermal conditions. At coating velocities of 0.05 to 0.1 cm/sec, large-grain layers were achieved having thicknesses in the 100 to 200 μm range. These layers display the same type of unidirectional solidification experienced in dip coating at these coating rates. Figure 11 is a photomicrograph of one of these layers which was coated at a substrate velocity of 0.95 cm/sec. The layer was 100 μm thick and had highly twinned single grains as large as 1.3 mm wide. A faster (0.23 cm/sec) grown coating, on the other hand, produced a larger (~35 cm^2) layer which was only 10 μm thick (see Figure 12). The grain structure here is also very similar to that of dip-coated layers grown under similar conditions.

We are encouraged by the fact that the most recent SCIM-coated layers do indicate that large-grain SOC sheet silicon is possible by this coating technique. The major obstacle to continuous coating remains to be this downstream overflow of molten silicon. An immediate effort will be made to correct the poor trough temperature uniformity which is a suspect for causing the problem. Should this fail to correct it, we are giving consideration to elevating the downstream end of the coater. The coater was designed to be tilted as much as 30 degrees above the horizon. A 30 degree tilt would provide a G/2 downward force on the molten silicon and by doing so could possibly render the temperature uniformity along the trough less critical. Such a change would require only minor modifications to the system.

In summary, we believe that the coating runs performed this reporting period clearly demonstrate that silicon can be coated onto ceramic in continuous manner. To do so in a routine fashion, however, will require much greater temperature uniformity and control than we originally had anticipated.

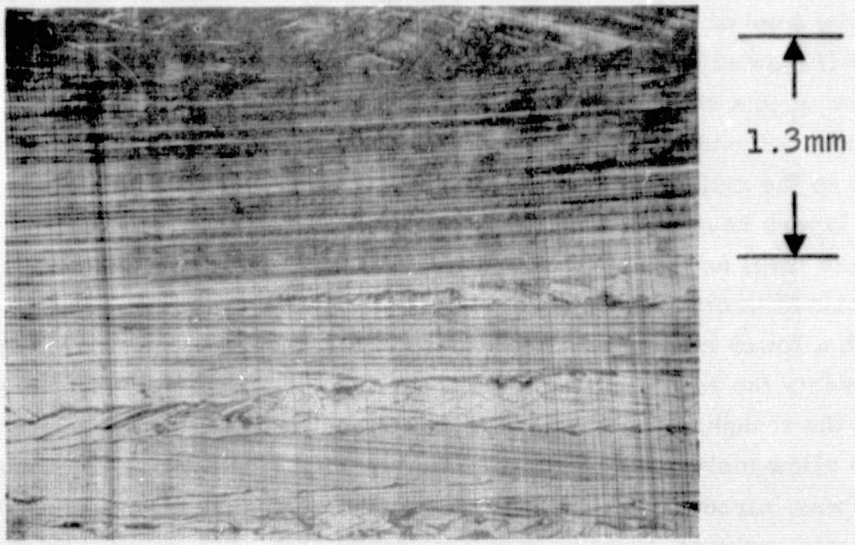

Figure 11. Photomicrograph of SCIM-Coated Layer Grown at 0.095 cm/sec

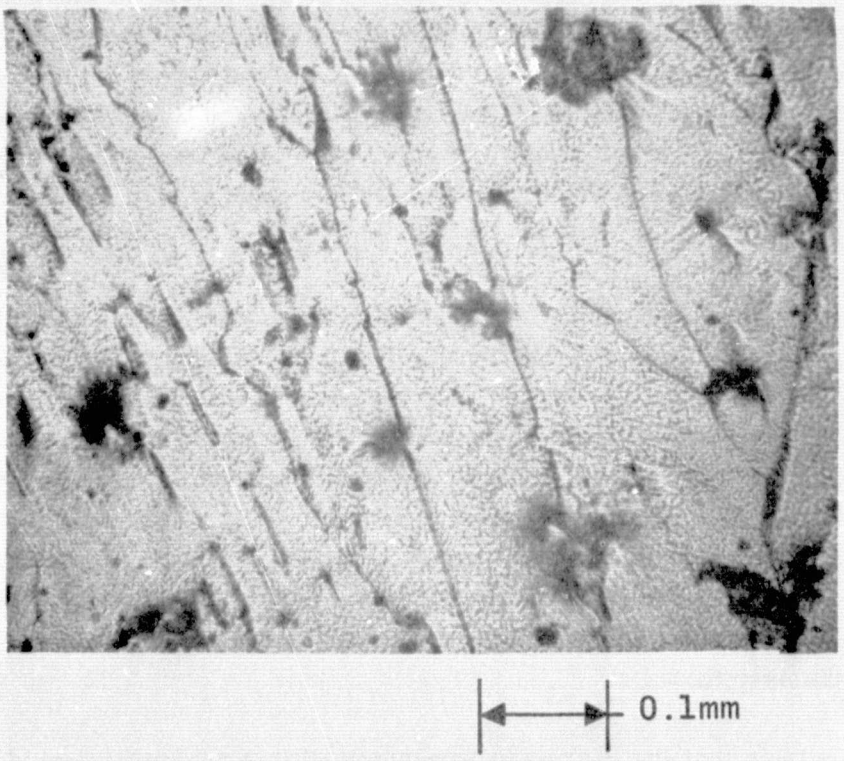

Figure 12. Photomicrograph of SCIM-Coated Layer Grown at 0.23 cm/sec

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CELL FABRICATION AND DEVELOPMENT (B. Grung, T. Heisler, S. Znameroski - Task II and Task VI)

Performance of SOC Cells

So far, the best SOC cell has a total-area conversion efficiency of 9.6 percent (AM1, ELH, AR), for a total area of 4.08 cm^2. The primary characteristics of this cell and 22 other recent SOC cells are given in Tables 3 and 4. The average conversion efficiency after AR coating is 8.3 percent, with a standard deviation of 0.8 percent. All efficiency values were measured using an ELH lamp and a new standard reference cell recently supplied by JPL. The height of the lamp was adjusted to give a light intensity of 100 mW/cm^2.

Table 3. Slotted SOC Cell Conversion Efficiency

Item	Cell No.	Total-Area Conversion Efficiency (%)	
		Before AR	After AR
1	143-12I	5.0*	6.1
2	143-12II	5.8*	7.1
3	143-13I	6.0*	9.2
4	143-13II	6.5*	9.0
5	144-4	6.1*	8.2
6	147-7	4.5	---
7	148-8T	5.9*	7.9
8	148-8	5.7*	7.8
9	148-15	4.4	---
10	148-16L	5.4	---
11	148-16R	6.4	---
12	146-6L	5.6*	9.6
13	146-6R	5.2*	7.8
14	148-7L	6.2	---
15	148-7R	6.9	---
16	151-10L	6.3	8.3
17	151-10R	6.6	8.4
18	151-13L	7.3	8.7
19	151-13R	6.6	9.0
20	151-14L	6.0	8.2
21	151-14R	6.3	8.6
22	151-15L	6.5	8.5
23	151-15R	5.9	8.2
Avg. Value	---	6.0(±0.7)	8.3(±0.8)

Note: The asterisk indicates values that could not be measured using the new standard cell from JPL. Such values were estimated from previous measurements.

Table 4. Slotted SOC Cell Performance Parameters

Cell No.	Diffusion No.	V_{oc} (V)	J_{sc} (mA/cm^2)	Fill Factor	Total-Area Conversion Efficiency (%)
143-12I	Q46	0.54	17.6*	0.62	5.0*
After AR coating		0.55	22.6	0.49	6.1 (AR)
143-12II	Q46	0.54	17.3*	0.62	5.8*
After AR coating		0.55	22.6	0.62	7.7 (AR)
143-13I	Q46	0.54	16.0*	0.70	6.0*
After AR coating		0.55	22.8	0.74	9.2 (AR)
143-13II	Q46	0.54	17.0*	0.71	6.5*
After AR coating		0.54	23.3	0.71	9.0 (AR)
144-4	Q46	0.54	16.7*	0.68	6.1*
After AR coating		0.55	23.7	0.63	8.2 (AR)
147-7	Q48	0.51	17.1	0.51	4.5
148-8T	Q48	0.53	15.9*	0.69	5.9*
After AR coating		0.54	21.6	0.68	7.9 (AR)
148-8	Q48	0.54	16.5*	0.64	5.7
After AR coating		0.54	22.8	0.63	7.8 (AR)
148-15	Q48	0.52	15.7	0.55	4.4
148-16L	Q48	0.53	15.8	0.65	5.4
148-16R	Q48	0.54	16.3	0.72	6.4
146-6L	Q51	0.55	18.1*	0.57	5.6*
After AR coating		0.55	23.6	0.74	9.6 (AR)
146-6R	Q51	0.53	16.1*	0.61	5.2*
After AR coating		0.54	22.5	0.65	7.8 (AR)
148-7L	Q51	0.54	17.5	0.65	6.2
148-7R	Q51	0.54	17.5	0.73	6.9
151-10L	Q53	0.53	16.5	0.72	6.3
After AR coating		0.54	21.6	0.70	8.3 (AR)
151-10R	Q53	0.54	16.6	0.74	6.6
After AR coating		0.54	21.5	0.72	8.4 (AR)
151-13L	Q52	0.53	18.7	0.73	7.3
After AR coating		0.54	23.0	0.69	8.7 (AR)
151-13R	Q52	0.54	17.1	0.72	6.6
After AR coating		0.55	22.8	0.71	9.0 (AR)
151-14L	Q52	0.53	16.8	0.67	6.0
After AR coating		0.54	22.8	0.67	8.2 (AR)
151-14R	Q52	0.54	16.8	0.70	6.3
After AR coating		0.54	23.2	0.68	8.6 (AR)
151-15L	Q53	0.54	17.4	0.70	6.5
After AR coating		0.54	23.4	0.67	8.5 (AR)
151-15R	Q53	0.54	16.6	0.66	5.9
After AR coating		0.55	23.3	0.64	8.2 (AR)

Note: All cells have a total area of 4.08 cm^2 and the metallization pattern covers 10 percent of the total area.

All recent SOC cells have a total area of 4.08 cm^2 and a metallization pattern that covers 10 percent of the total area. The cells use slotted mullite-based substrates. The slots provide a way for making electrical contact to the back side of the silicon layer. The mullite-based material has a thermal expansion coefficient that closely matches that of silicon.

The current-voltage characteristics of the best cell are given in Figure 13. This cell has an open-circuit voltage, V_{oc}, of 0.55 V, a total-area short-circuit current density, J_{sc}, of 23.6 mA/cm^2, a fill-factor (FF) of 0.74, and (as already noted), a total-area conversion efficiency of 9.6 percent (AM1, ELH, AR). The active-area short-circuit current density is $\sim$ 26 mA/cm^2, which is typical of most recent cells (see below).

Performance of Single-Crystal Cells

The primary characteristics of 10 recent single-crystal cells are given in Table 5. The best cell has a total-area short-circuit current density (J_{sc}) of 30.7 mA/cm^2, an open-circuit voltage (V_{oc}) of 0.58 V, a fill-factor (FF) of 0.77, and a total-area conversion efficiency of 13.7 percent (AM1, ELH, AR), for a total area of 4.08 cm^2.

Average Values

Table 6 summarizes the data given in Table 4 for SOC cells and in Table 5 for single-crystal cells. Table 6 gives average values for the various cell characteristics, along with standard deviation values. A comparison of SOC cells with single-crystal cells shows the following: With an antireflection coating, the SOC cells have (1) an average short-circuit current density that is about 36 percent lower, (2) an average open-circuit voltage that is about 6 percent lower, and (3) an average fill factor that is about 10 percent lower. Thus, the area which offers the greatest improvement potential in SOC cells is the short-circuit current density.

Short-Circuit Current-Density Values of Recent SOC Cells

Recent J_{sc} values have been remarkably consistent, which indicates that the silicon material properties have been quite uniform. As Table 4 shows, 23 cells have been fabricated from six different dip-coating runs (runs No. 143, 144, 146, 147, 148, and 151). Some of the substrates were coated early in a run; others, late. In spite of such fabrication differences, the active-area J_{sc} values were spread over a very narrow range -- the lowest value was 23.7 mA/cm^2; the highest value, 26.1 mA/cm^2. The average value was 25.1 mA/cm^2, with a standard deviation of 0.7 mA/cm^2. Thus, for six separate dip-coating runs, the J_{sc} values have been within about 3 percent of the average value.

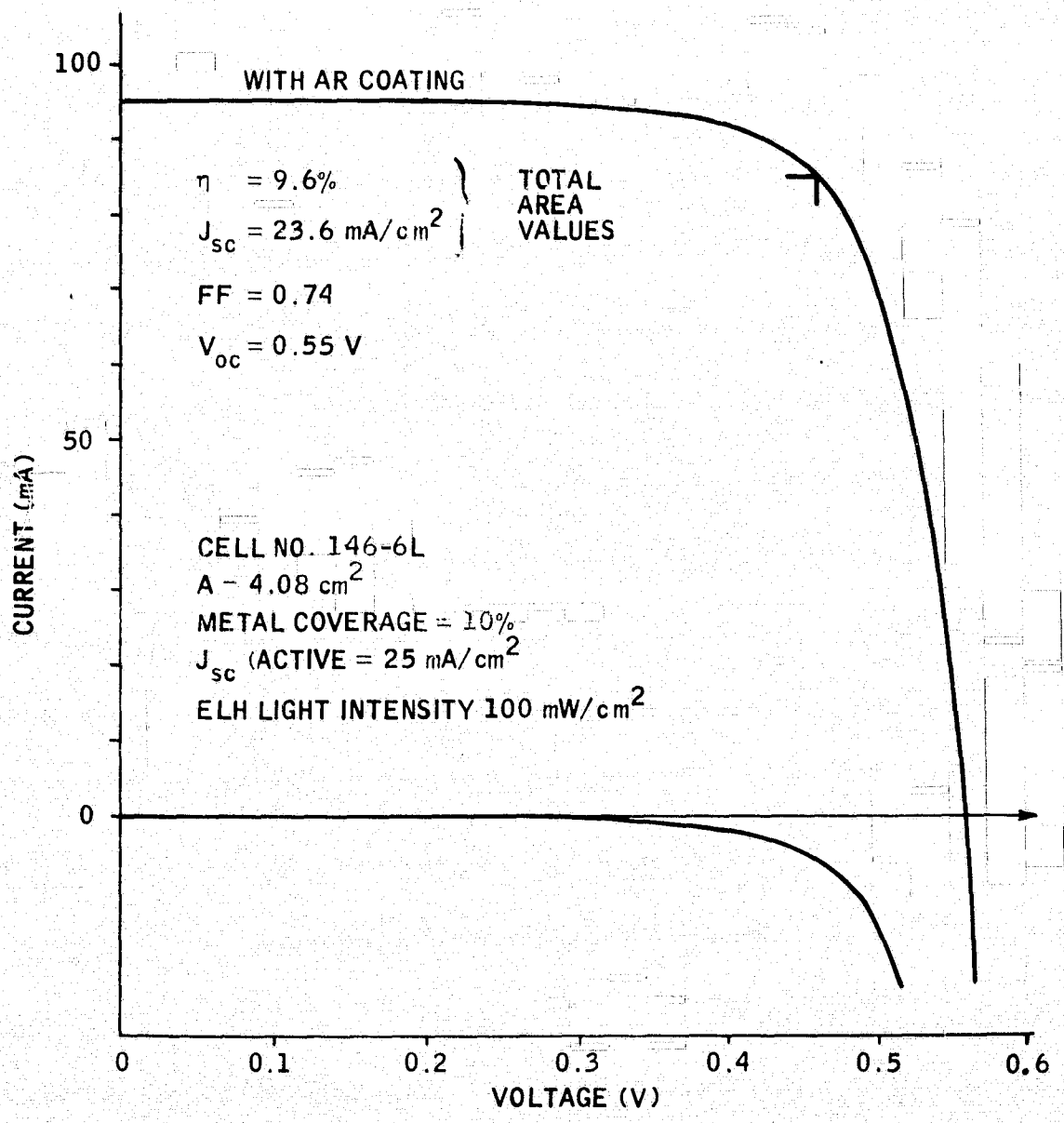


Figure 13. Current-Voltage Characteristics of Cell No. 146-6L

Table 5. Single-Crystal Cell Performance Parameters

Cell No.	V_{oc} (V)	J_{sc} (mA/cm^2)	Fill Factor	Total-Area Conversion Efficiency (%)
Q52I	0.56	22.0	0.79	9.7
After AR coating	0.56	31.5	0.75	13.3 (AR)
Q52II	0.55	21.2	0.76	8.9
After AR coating	0.56	31.5	0.71	12.6 (AR)
Q51BI	0.56	21.9*	0.80	9.8*
After AR coating	0.58	30.7	0.77	13.7 (AR)
Q51BII	0.56	28.2*	0.78	9.5*
After AR coating	0.57	30.5	0.76	13.2 (AR)
Q51AI	0.56	20.9*	0.79	9.3*
After AR coating	0.57	30.6	0.75	13.1 (AR)
Q51AII	0.56	20.5*	0.78	8.9*
After AR coating	0.56	30.1	0.75	12.6 (AR)
Q48BI	0.57	21.2*	0.77	9.2*
After AR coating	0.57	31.3	0.74	13.3 (AR)
Q48BII	0.56	22.4*	0.74	9.2*
After AR coating	0.55	30.8	0.71	12.1 (AR)
Q48AI	0.57	21.1*	0.79	9.4*
After AR coating	0.57	30.9	0.76	13.5 (AR)
Q48AII	0.57	20.5*	0.78	9.1*
After AR coating	0.57	31.4	0.74	13.5 (AR)

Note: The asterisk indicates values that could not be measured using the new standard cell from JPL. Such values were estimated from previous measurements.

Table 6. Performance Parameter Average Values

Parameter	SOC Cells		Single-Crystal Cells	
	Before AR	After AR	Before AR	After AR
J_{sc} (mA/cm^2):				
Active area	18.5 (±0.8)	25.1 (±0.7)	24.2 (±2.3)	34.0 (±0.5)
Total area	16.9 (±0.8)	22.8 (±0.7)	22.0 (±2.3)	30.9 (±0.5)
V_{oc} (V)	0.54 (±0.01)	0.54 (±0.01)	0.56 (±0.01)	0.57 (±0.01)
Fill factor	0.66 (±0.06)	0.67 (±0.06)	0.78 (±0.02)	0.74 (±0.02)
Total area η (%)	6.0 (±0.7)	8.3 (±0.8)	9.3 (±0.3)	13.1 (±0.5)

NOVEL DEVICE DEVELOPMENT (B. Grung, S. Znameroski - Task VI)

Five 2X cells have been completed. Table 7 gives the primary characteristics of each cell before an AR coating was deposited and before the integral optical coupler (IOC) was attached. The best cell (No. 151-1) had an active-area conversion efficiency of 6.0 percent (AM1, no AR), for an active area of 4.2 cm^2. This cell, as well as all other 2X cells, contains five separate sections connected in series.

Table 7. Performance Parameters of 2X-Cells Without IOC Devices

Ident.	Cell No.	Active Area (cm^2)	V_{oc} (V)	Fill Factor	J_{sc} (mA/cm^2)	Active-Area Conversion Efficiency (%)
1	126-2	0.84	0.49	0.56	19.9	5.4
2	128-8	0.84	0.48	0.54	18.9	4.8
3	186-3	0.84	0.48	0.48	17.1	3.9
4	139-10	0.84	0.45	0.54	17.5	4.2
5	151-1	0.84	0.50	0.57	21.2	6.0
6	Single crystal	0.84	0.55	0.66	27.6	10.0

An AR coating was deposited on the three middle sections of cell No. 126-2, and an IOC was then attached. The primary characteristics of the three middle sections are given in Table 8, for the three experiments conditions (before AR and IOC, after AR but before IOC, and after AR and IOC). Table 8 shows that the active-area short-circuit current density of a section is increased by a factor of about 1.38 when an AR coating is used and by a factor of about 2.28 when both an AR coating and an IOC concentrator are used. The concentrator was designed to increase J_{sc} by a factor of 2.

These results indicate the IOC concept is viable. Further work must be done in the area of stripe cell fabrication and IOC alignment in order to improve the overall performance of the IOC/SOC device.

Table 8. Performance Parameters of Non-Slotted SOC Cell (No. 126-2)

Section No.		V_{oc} (V)	Fill Factor	Total Area J_{sc} (mA/cm^2)	Total Area η (%)	Active Area J_{sc} (mA/cm^2)	Active Area η (%)
2	No AR or IOC	0.49	0.56	9.4	2.6	21.1	5.8
	With AR	0.49	0.53	13.6	3.4	29.3	7.5
	With both	0.51	0.42	22.2	4.7	49.4	10.4
3	No AR or IOC	0.48	0.53	9.5	2.4	21.2	5.3
	With AR	0.48	0.48	12.9	3.0	28.8	6.6
	With both	0.50	0.36	21.1	3.8	47.0	8.5
4	No AR or IOC	0.47	0.56	9.4	2.5	20.8	5.5
	With AR	0.48	0.53	12.5	3.2	27.9	7.1
	With both	0.50	0.43	21.3	4.5	47.5	10.0
All three sections connected in series, with AR and IOC		0.50	0.39	21.0	4.1	46.7	9.0

BACK SURFACE FIELD METALLIZATION (T. Schuller)

The development of a process for the formation of a BSF on the SOC material continued during the quarter. Emphasis was placed first on achieving this effect with the single-crystal wafers. Several changes in processing were initiated as a result of discussions with Frank Uno of JPL. These changes are as follows:

- A minimum of 5 minutes air dry was used after screening on aluminum paste (200-mesh screen).
- A higher-resistivity P-doped silicon was used.
- The bake temperature was decreased from 200 to 225°C and the bake time reduced to 10 minutes.
- The furnace temperature was increased to 880°C or 900°C (880°C is presently used, because the aluminum on the back is not removed).

- The gas mixture was changed from argon/oxygen to nitrogen/oxygen in the ratio of 80% N_2 and 20% O_2.
- The gas flow was reduced to ~ 1000 cc/minute in a furnace tube of 2-1/8-inch ID. This parameter will be varied.
- A new furnace boat was fabricated so that the wafers are vertical.
- The time in the furnace was reduced to 10 seconds (no warmup, in and out fast).

The foregoing changes were made, and diodes processed on two single-crystal wafers with 11 ohm-cm resistivity. One wafer was 16 mils thick and the other etched to 9 mils thickness. The resulting V_{oc} of diodes processed on the wafers was low. See Tables 9 and 10.

Table 9. V_{oc} in 16-Mil-Thick Wafer

- Furnace temp = 880°C
- Time = 10 sec
- 80% N_2, 20% O_2
- Gas flow rate = 1880 cc/min

Diode	V_{oc} (V)
1	0.53
2	0.53
3	0.52
4	0.52
5	0.52
6	0.52
7	0.52
8	0.52

Table 10. V_{oc} in 9-Mil-Thick Wafer

- Furnace temp = 882°C
- Time = 8 sec
- 81% N_2, 19% O_2
- Gas flow rate = 1050 cc/min

Diode	V_{oc} (V)
1	0.51
2	0.52
3	0.51
4	0.52
5	0.53
6	0.50
7	0.52
8	0.52
9	0.52

All wafers processed to date used an in-house aluminum paste. A commercial paste (Engelhard A-3484) has been purchased. This next quarter both single-crystal and SOC material will be processed using the new paste and varying the gas flow rate. A second parameter to be varied will be the oxygen concentration.

SHAPE OF LIQUID - SOLID INTERFACE (D. Zook and C. Pickering)

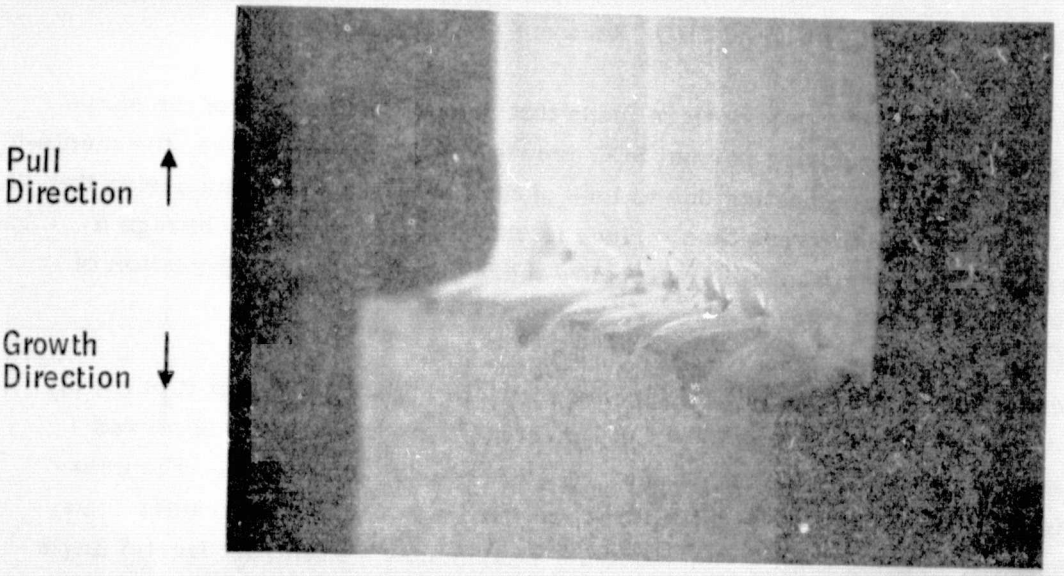
During the quarter, some observations were made that provide indications of the shape of the liquid - solid interface during normal SOC growth. On a few occasions, the meniscus has broken suddenly during coating due to loss of the hand-rubbed carbon during the soak period. An example of the resultant surface is shown in Figure 14. Although a completely clean decant of the liquid did not occur, there is a very clear suggestion of the shape of the liquid - solid interface.

The main feature of the liquid - solid interface as shown in Figure 14 is that it is nearly perpendicular to the growth direction. This is expected on the basis of the observed similarities between SOC growth and EFG growth, as previously discussed. The unexpected result is that the surface is slightly tilted away from the substrate, rather than toward the substrate. Tilting toward the substrate would cause a reentrant (acute) angle at the edge of the silicon, and would explain the apparent good features of SOC growth (e.g., the tendency of SiC particles to accumulate at the ceramic surface rather than the free surface). An interface tilted toward the substrate was expected on the basis of simple thermal modeling that did not accurately take into account the two-dimensional nature of the heat flow.

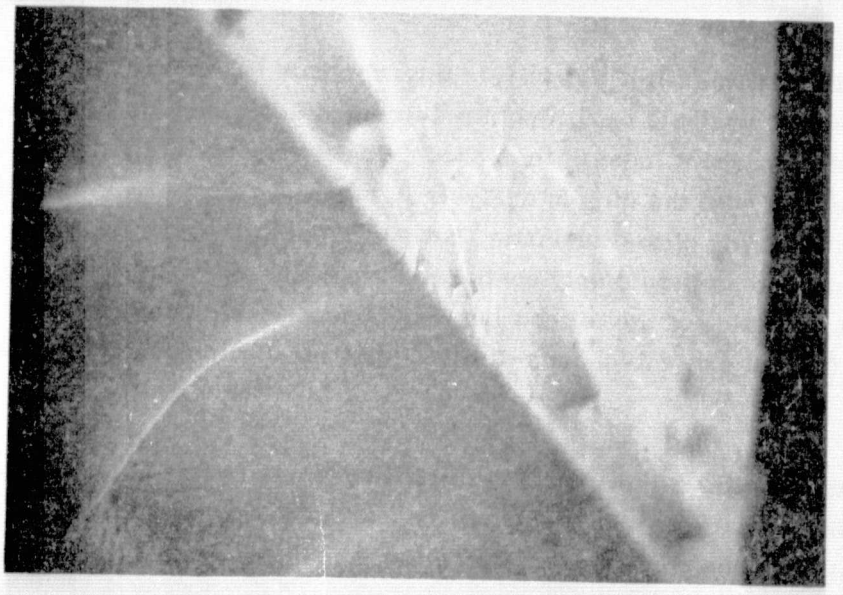
A liquid - solid interface tilted away from the substrate is, in fact, predicted by the more exact thermal analysis by S. Schuldt described elsewhere in this report. It is interesting that throughout most of the silicon, the isotherms are tilted toward the substrate in agreement with the simple analysis (i.e., heat flow is from the ceramic to the silicon). In the vicinity of the interface, however, the heat flows from the silicon to the ceramic because the hot liquid only coats one side of the substrate. In this area, heat flow at the ceramic side of the silicon layer is conduction-limited, whereas on the free surface, heat flow is current-density-limited (or area-limited) by the Stefan-Boltzmann law.

The shape of the liquid - solid interface described above has been indicated on the two samples on which a carbon-free meniscus break was observed. Visual observations clearly indicate that the surface is concave, as demanded by theory, although the concavity is not evident in Figure 14.

During the quarter, some observations were made that suggest relationships between the heat transfer, the angle of the liquid - solid interface, and the necessary conditions for growth. During dip coating, one of the unslotted substrates broke and fell back into the melt. An unslotted substrate was used to draw it out. This frequently can be done



(a) 50x SEM image showing over-all shape of surface from which the liquid silicon suddenly pulled away.



(b) Magnified (200x) image showing twin boundaries and detailed surface shape. The sharp edge was at the triple (liquid-solid-vapor) junction during growth.

Figure 14. Shape of As-Grown SOC in the Vicinity of a Triple Junction

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because of the surface tension of the silicon which tends to hold the substrates together. The substrates were withdrawn at a constant velocity, with the carbon-coated side of the unbroken substrate away from the broken substrate. The result is that on a large region of the substrate, there is a thick layer of silicon on the back holding the two substrates together.

The resulting coating on the silicon is quite interesting. In the region where there is no silicon on the back, the layer appears quite smooth with the normal twinned texture. In the regions where there was silicon on the back, however, the silicon layer on the front is quite rough. Microscopic examination shows that the crystal structure in this region consists of fine-grain silicon. A surprising result is that the surface is covered with a high density of SiC particles visible only at high magnification. The SiC particles normally appear at the silicon - ceramic interface and we have never observed them on the as-grown surfaces of normally twinned silicon.

Calculation and Observation of Meniscus Shape

The shape of the liquid meniscus in our model of SOC growth is shown in Figure 15. The coordinate system shown in Figure 15 is chosen so that x = 0 is the plane of the wall and y = 0 is the surface of the liquid far away from the meniscus. The shape of a two-dimensional semi-infinite liquid bounded by a rigid plane wall is well known from hydrostatics. A derivation of the differential equation and its solutions is given by McNutt and Andes.[3] The radius of curvature, R, of the liquid meniscus is given by

$$\frac{1}{R} = \frac{\frac{d^2y}{dx^2}}{\left[1 + \left|\frac{dy}{dx}\right|^2\right]^{3/2}} = \frac{\frac{d^2x}{dy^2}}{\left[1 + \left|\frac{dx}{dy}\right|^2\right]^{3/2}} = \frac{y}{K^2} \qquad (1)$$

where $K^2 = \gamma_L/\rho_L g$ and γ_L is the surface tension of silicon (720 dynes/cm), ρ_L is the density of the liquid (2.53 g/cm^3), and g is the acceleration of gravity (980 cm/sec^2). The solution with the appropriate boundary conditions is given by:

$$x = K\left\{\cosh^{-1}\frac{2K}{y} - 2\sqrt{1 - \left|\frac{y}{2K}\right|^2}\right\} - K\left\{\cosh^{-1}\frac{2K}{h_o} - 2\sqrt{1 - \left|\frac{h_o}{2K}\right|^2}\right\} \qquad (2)$$

where $h_o^2 = 2K^2(1 - \sin\theta_c)$ is the meniscus height which depends on the contact angle, θ_c. The solution is plotted to scale in Figure 15, which also shows the typical dimensions of a slotted substrate which is 1 mm thick, having 1-mm horizontal slots, on 1.5-mm centers.

On the noncarbon-coated back side of the ceramic, it is assumed that the silicon - ceramic contact angle is 90 degrees and meniscus height is zero, as in Figure 15. Observations of the back side during actual growth show that the average contact angle is indeed 90 degrees but that slight positive and negative fluctuations continuously occur as the substrate is withdrawn. As a slot approaches the liquid level, the black meniscus attaches itself to the slot. After the slot rises, the meniscus breaks and goes back to the 90-degree contact and this breaking of the meniscus causes motion of the substrate resulting in horizontal striations visible on slotted substrates.

The calculated meniscus height depends on the surface tension and the contact angle. In Figure 15, a contact angle of 11 degrees is assumed, as measured by Surek.[4] Although we have not yet been able to measure the meniscus shape and contact angle in detail, we find that the meniscus height is about 6.5 mm and appears to be independent of growth speed and melt temperature over the range of speeds and temperatures investigated. This is in agreement with Surek's observations[4] that the steady-state contact angle is independent of velocity and temperature gradients over a wide range.

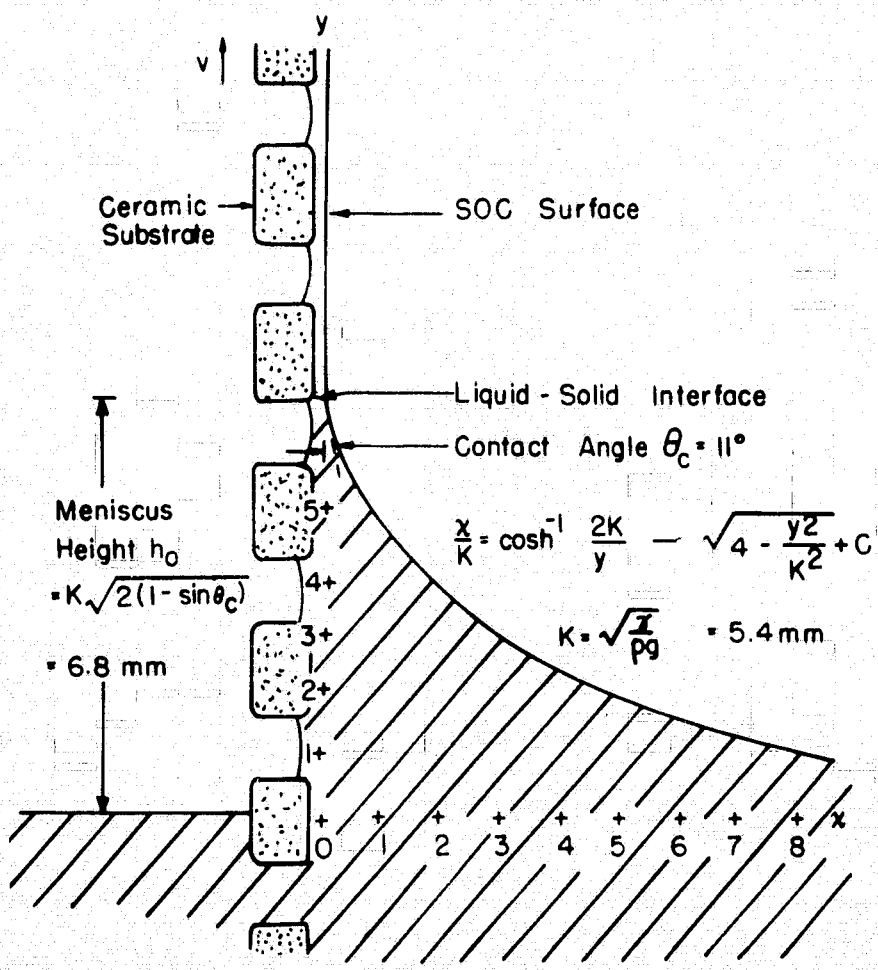


Figure 15. Scale Representation of SOC Growth. The horizontal and vertical scales are in millimeters. The calculated meniscus shape is based on thermal equilibrium.

THERMAL ANALYSIS OF THE VERTICAL SILICON-ON-CERAMIC GROWTH PROCESS (S. B. Schuldt)

Introduction

Sheet silicon may be grown vertically from the melt either unsupported[5-10] or attached to a substrate material.[11-14] In either case, the attainable growth rate is limited by heat extraction efficiency. The steady-state analysis of unsupported silicon growth is greatly simplified by the symmetry of the structure, leading to uncomplicated solution to the heat equations.[13] Important by-products of the analysis are expressions for pull speed versus sheet thickness and for the shape of the crystallization or freezing front. This symmetry does not exist in the case of silicon grown on ceramic, and numerical methods were chosen to solve the heat equations.

The essential features of dip coating SOC are shown in Figure 16. Ceramic wafers are pulled vertically from the silicon melt at constant speed, v. The freezing front

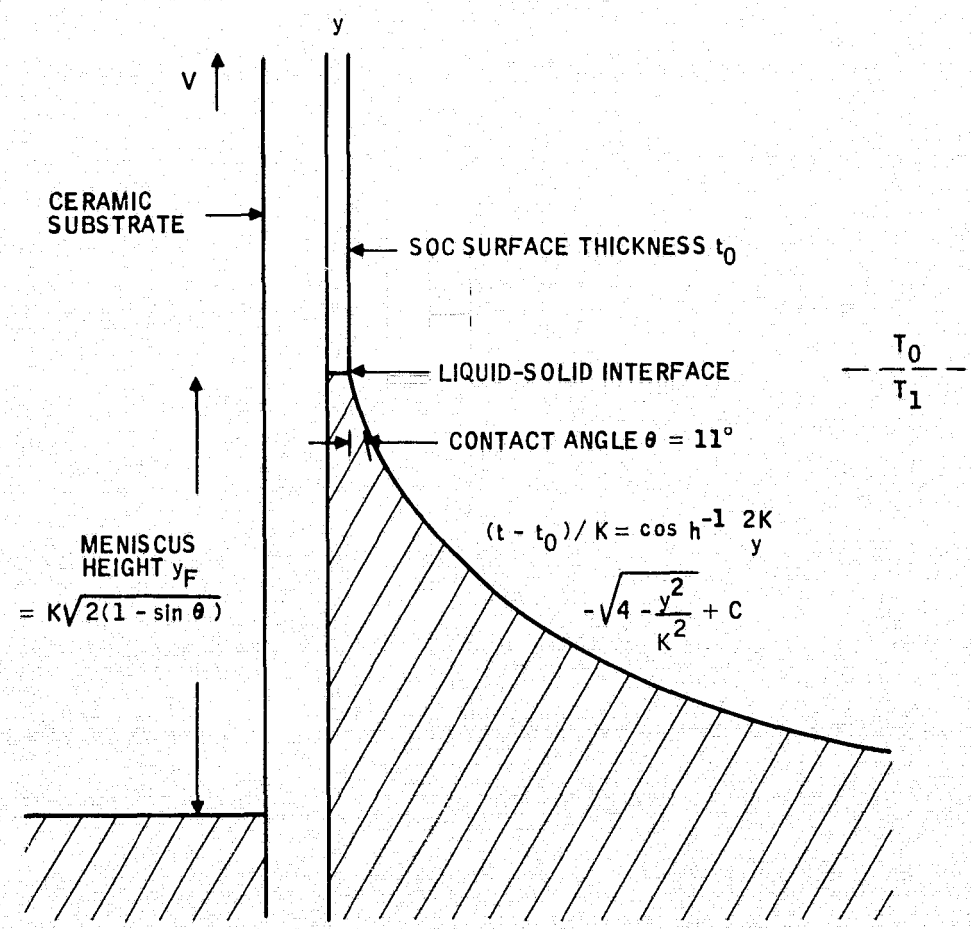


Figure 16. Cross-Section View of SOC Growth. The meniscus shape is based on hydrostatic equilibrium. Radiative background temperatures T_0 and T_1 are seen above and below the liquid - solid interface, respectively.

appears at a height y_F above the melt. The value of y_F at zero pulling speed may be calculated from hydrostatic considerations.[10] Moreover, this appears to remain unchanged in actual steady-state growth for pulling speeds up to well into the millimeter-per-second range.[14] Above y_F, the temperatures in the structure begin to fall toward some effective radiation temperature, T_o, of the environment. A possibly different radiation temperature, T_1, is seen by the portion of the structure below the freezing front. In the present study, only radiative heat removal was considered and the temperatures T_1 and T_o were assumed uniform over $0 \le y < y_F$ and $y_F \le y < \infty$, respectively. The simple two-part background is used to give a crude approximation to the effect of a heat shield located at y_F. More general heat loss functions are easily incorporated and may be investigated later. As was true in the unsupported case, the rate of heat extraction by radiation must balance the rate of removal of sensible heat from the melt (by convection) plus the rate of release of latent heat at the freezing front. In the present case, most of the sensible heat is carried in the ceramic.

Heat Equations

Two zones are identified because of the different thermal properties of molten and solid silicon. In the zone $y_F \le y < \infty$, the steady-state heat equations in the ceramic portion follow from two-dimensional heat balance, including convective terms:[15]

$$\frac{\partial}{\partial x}\left(k_c \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k_c \frac{\partial T}{\partial y}\right) - \rho_c C_c v \frac{\partial T}{\partial y} = 0 \quad 0 \le x \le t_c \tag{3}$$

$$k_c \frac{\partial}{\partial x} T(0,y) = \varepsilon_c \sigma\left\{\left[T(0,y)\right]^4 - T_o\right\}^4 \tag{4}$$

$$T(x,\infty) = T_o \tag{5}$$

The two-dimensional model is appropriate because the width of the structure (z-dimension) is assumed large compared with the thickness, $t_c + t_o$. Physical parameters are identified in Table 11. For the silicon portion, a one-dimensional temperature profile, $U_o(y)$, is used, equivalent to assuming the isotherms are horizontal. This assumption will be checked below by estimating the inclination of the isotherms in the solid silicon portion. The steady-state equations in the solid silicon ($y \ge y_F$) are

$$t_o\left\{\frac{d}{dy}\left(k_o \frac{dU_o}{dy}\right) - \rho_o C_o v \frac{dU_o}{dy}\right\} = f_o(y) \tag{6}$$

$$f_o(y) = \varepsilon_o \sigma\left\{\left[U_o(y)\right]^4 - T_o^4\right\} - k_c \frac{\partial}{\partial x} T(t_c, y) \tag{7}$$

Table 11. Nomenclature and Numerical Data

Symbol	Description	Value/Units
C_c	Specific heat of ceramic	1.04 (J/g °K)
$C_o \simeq C_1$	Specific heat of silicon	0.954 (J/g °K)
$J_o(y)$	Silicon heat flux density ($y > y_F$)	(W/cm^2)
$J_1(y)$	Silicon heat flux density ($y < y_F$)	(W/cm^2)
k_c	Heat conductivity of ceramic	0.041 (W/cm °K)
k_o	Heat conductivity of solid silicon	$343/U_o$ (W/cm °K)
k_1	Heat conductivity of liquid silicon	0.6 (W/cm °K)
L	Latent heat of fusion of silicon	1802 (J/g)
T(x, y)	Ceramic temperature	(°K)
T_o	Downstream ($y > y_F$) ambient temperature	(°K)
T_1	Upstream ($y < y_F$) ambient temperature	(°K)
T_M	Melt temperature	(°K)
T_F	Silicon freezing temperature	1685 (°K)
t_c	Ceramic thickness	(cm)
t_o	Solid-silicon layer thickness	(cm)
$t_1(y)$	Liquid-silicon layer thickness	(cm)
$U_o(y)$	Silicon temperature ($y \geq y_F$)	(°K)
$U_1(y)$	Silicon temperature ($y \leq y_F$)	(°K)
v	Pull speed	(cm/sec)
y_F	Total meniscus height above melt	0.5 or 0.69 (cm)
δ	Numerical grid spacing	0.02 (cm)
ρ_c	Ceramic density	3.3 (g/cm^3)
$\rho_o \simeq \rho_1$	Silicon density	2.33 (g/cm^3)

$$U_o(y) = T(t_c, y) \tag{8}$$

$$U_o(y_F) = T_F \tag{9}$$

The extraction term $f_o(y)$ includes both radiation at the external surface and conduction across the internal surface into the ceramic.

In the zone $0 \leq y < y_F$, the equations for the ceramic portion are similar to Equations (3), (4), and (5), except for the radiation temperature, T_1, in place of T_o (Figure 16) and a boundary condition at $y = 0$ instead of $y = \infty$:

$$\frac{\partial}{\partial x}\left(k_c \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k_c \frac{\partial T}{\partial y}\right) - \rho_c C_c v \frac{\partial T}{\partial y} = 0 \tag{10}$$

$$k_c \frac{\partial}{\partial x} T(0,y) = \varepsilon_c \sigma\left\{\left[T(0,y)\right]^4 - T_1^4\right\} \tag{11}$$

$$T(x,0) = T_M \tag{12}$$

In the liquid-silicon portion, the variable thickness t_1 must be taken into account. The following is derived based on the assumption of horizontal isotherms [see next subsection for full derivation of Equation (13)]:

$$\frac{d}{dy}\left(t_1 k_1 \frac{dU_1}{dy}\right) - \rho_o v t_o C_1 \frac{dU_1}{dy} = f_1(y) \tag{13}$$

$$f_1(y) = \left\{1 + \left[\frac{dt_1}{dy}\right]^2\right\}^{1/2} \varepsilon_1 \sigma\left\{\left[U_1(y)\right]^4 - T_1^4\right\} - k_c \frac{\partial}{\partial x} T(t_c, y) \tag{14}$$

$$U_1(y) = T(t_c, y) \tag{15}$$

$$U_1(y_F) = T_F \tag{16}$$

A final condition expresses the fact that the freezing front is the source of a heat flux density (vertical component) equal to $\rho_o vL$:

$$-k_1 \frac{d}{dy} U_1(y_F) + \rho_o vL = -k_o \frac{d}{dy} U_o(y_F) \tag{17}$$

Derivation of Equation (13)

Refer to Figure 17. We assume horizontal isotherms so that temperature can be denoted $U_1(y)$. Vertical mass flow, independent of y, is equal to $\rho_o\, vt_o$. If $t_1(y)$ denotes local thickness, vertical heat flux, H(y), per unit width is

$$H(y) = \rho_o\, vt_o C_1 U_1 - t_1 k_1 dU_1/dy \tag{18}$$

Denoting by $f_1(y)$ the heat flux density lost by radiation at the curved surface and by condution to the ceramic, we then have

$$dH/dy + f_1 = 0$$

or

$$\frac{d}{dy}\left(t_1\, k_1 \frac{dU_1}{dy}\right) - \rho_o\, vt_o C_1 \frac{dU_1}{dy} = f_1(y) \tag{19}$$

For $t_1(y)$, we use the result from Harrill, et al:[10]

$$(t_1 - t_o)/K = \cos h^{-1}(2K/y) - \cos h^{-1}(2K/y_F)$$

$$+ \left[4 - (y_F/K)^2\right]^{1/2} - \left[4 - (y/K)^2\right]^{1/2} \tag{20}$$

where $K/y_F = [2(1 - \sin 0)]^{-1/2} = 0.79$ if the contact angle, θ, is 11 degrees.

Finite Difference Model

A finite two-dimensional array of points was chosen (Figure 18) as the framework to approximate the solution of the above equations by finite differences. The ceramic thickness is covered by four full-distance increments, δ, and two half-increments, $\delta/2$, making a total of five; hence, $\delta = t_c/5$. The same increment is used for the vertical direction. An integer, m_F, labels the approximate location, y_F, of the freezing front, separating the liquid and solid silicon phases. If m = 0 denotes the bottom row of points, the correspondence between m and y is

$$y = (m - 1/2)\,\delta \tag{21}$$

and m_F is the largest integer contained in $(y_F/\delta + 1)$.

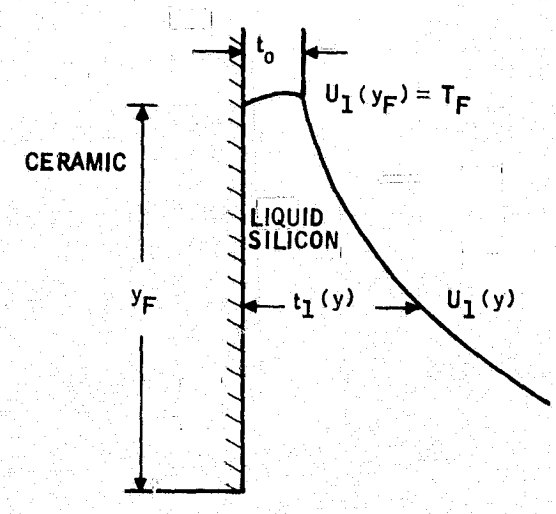


Figure 17. Diagram of Meniscus Region

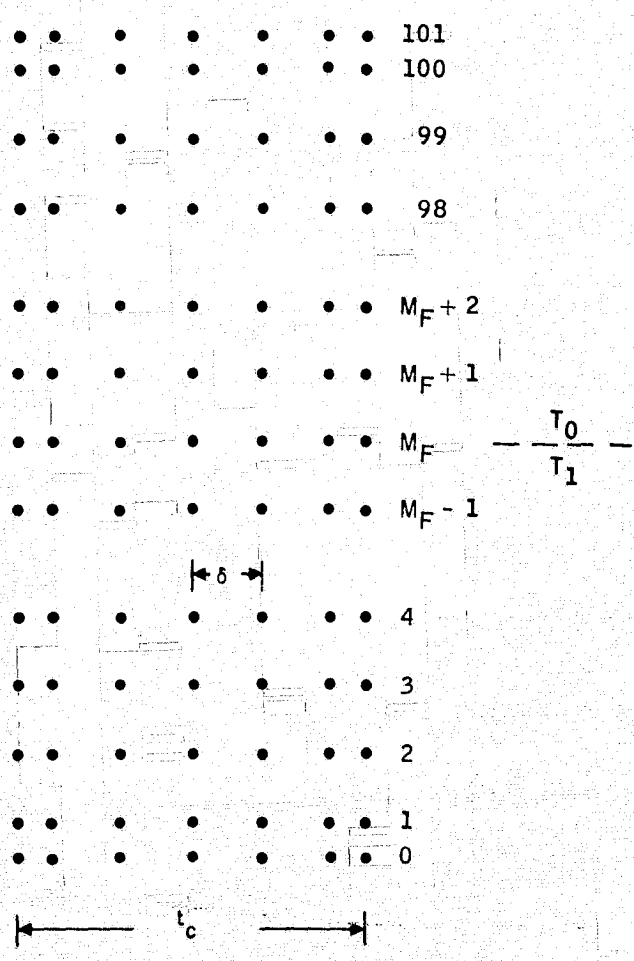


Figure 18. Finite Difference Array for Calculating SOC Temperature Profile. Right-hand column of points corresponds to silicon layer (one-dimensional approximation) and right-hand edge of substrate. The rest of the points represent locations within and at the left-hand edge of the substrate.

The right-hand column of points is sufficient to represent the entire silicon thickness due to our assumed horizontal isotherms. There are no discontinuities in the two-dimensional temperature profile; hence, the silicon temperatures are equal to the ceramic temperatures at the silicon - ceramic interface.

The details of the solution technique, a modified over-relaxation method (Gauss-Seidel)[16] are omitted here. The equations are nonlinear due to the Stefan-Boltzmann relations and the temperature-dependent k_o. For the latter, an approximate inverse temperature dependence, $k_o = 343/U_o$, is inferred from recommended data over the range $800°K \leq V_o \leq 1685°K$.[18] These nonlinearities are handled by means of coefficient updates at each Gauss-Seidel iteration.

The steady-state temperature profile depends on the thicknesses of ceramic and silicon, the pull speed, the melt temperature, and the background temperatures, T_o and T_1. Of course, T_F is fixed at 1685°K. Not all of the foregoing can be independently specified, since the problem would be overdetermined and a solution would, in general, be non-existent. As a mathematical convenience, we have chosen the melt temperature to be a dependent variable, and this is therefore an output of the calculation along with the temperature profile. Also, we specify the temperature differences $T_M - T_o$ and $T_M - T_1$ rather than T_o and T_1 directly (e.g., $T_M - T_1 = 1385°K$ will result in T_o being a little above room temperature because T_M will generally be a few degrees above 1685°K.

Interpretation

At the present time, the complete temperature profiles in ceramic and silicon are of only casual interest. Isotherms obtained by interpolation of output data of two computer runs are shown in Figure 19. The sparse, sharply-bent isotherms below the freezing front, and the sudden increase in isotherm density above the point of latent heat release, are features found in all the runs.

On the other hand, the silicon part of the profile is crucial and gives the nucleus of information for our interpretation of thickness versus growth speed. As in the case of unsupported silicon sheet growth,[13] a major assumption here is that stable growth of silicon on ceramic requires the liquid meniscus to be at or above the freezing temperature; that is, heat flow in the liquid must not be away from the freezing front. A condition for the limiting stable growth rate is that the temperature gradient on the liquid side of the interface approach zero. According to Brice,[17] maximum silicon thickness at a given velocity may be obtained by adjusting the melt temperature to a point just above the value where the interface becomes unstable and dendritic growth develops. In a computer calculation this would correspond to zero temperature gradient in the liquid at $y = y_F$.

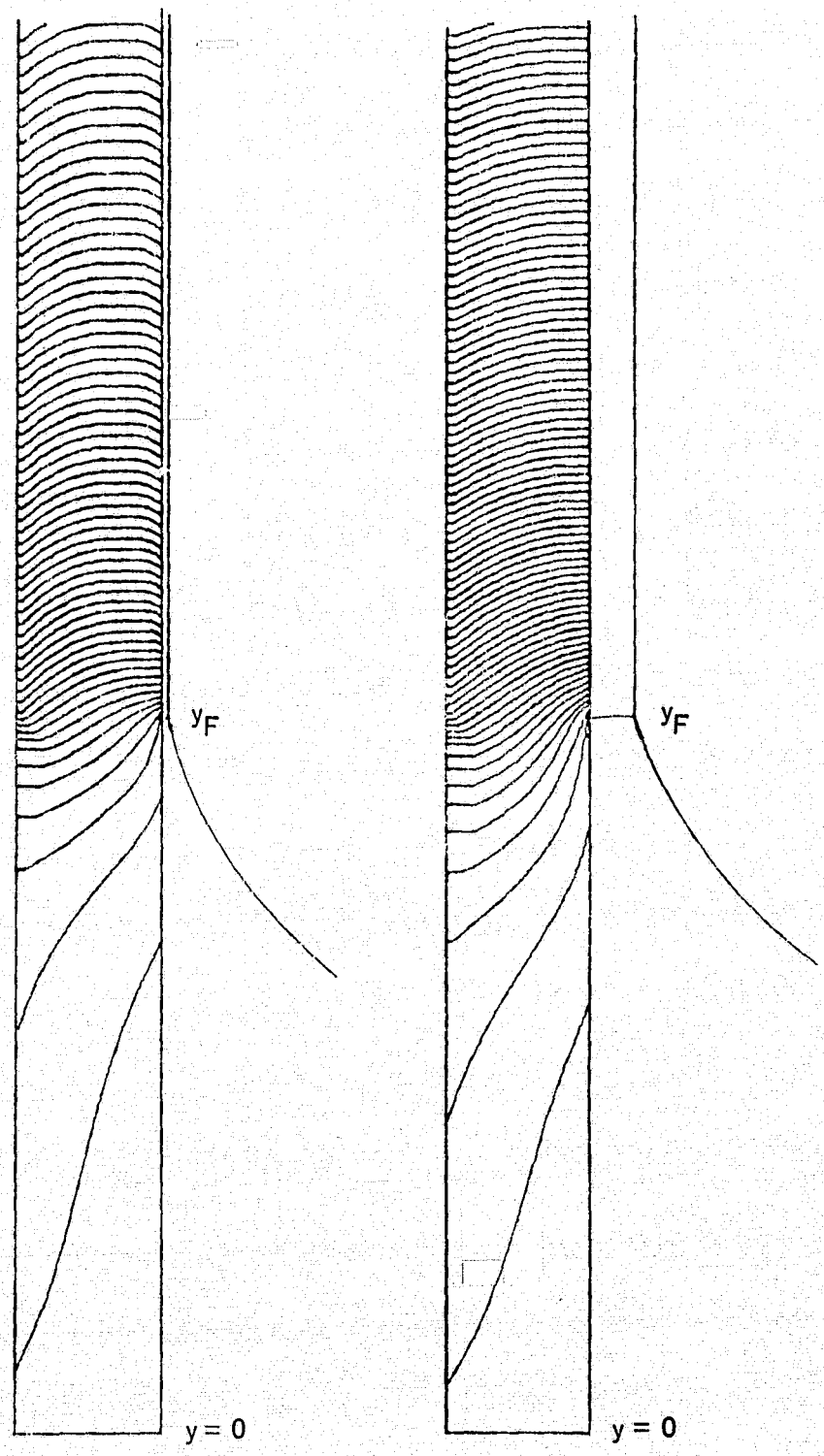


Figure 19. Isotherms for $T = T_M - 5n$, $n = 1, 2, \ldots$, by Two-Dimensional Interpolation; $t_c = 0.1$ cm, $y_F = 0.5$ cm, $T_M - T_o = 1385°K$, $T_M - T_1 = 300°K$. Left: $t_o = 0.003$ cm, $v = 0.153$ cm. Right: $t_o = 0.03$ cm, $v = 0.0685$ cm.

Figure 20 shows calculated normalized heat flux, $Jt/\rho v L t_o$, as a junction of y, where

$$J = J_1 = -k_1 \frac{dU}{dy} \quad \text{(liquid)} \tag{22}$$

$$J = J_o = -k_o \frac{dU}{dy} \quad \text{(solid)} \tag{23}$$

for three melt temperatures at the same pull speed. In Figure 20, the middle case (II) gives maximum stable t_o because $J_1(y_F) = 0$. Case I, with a higher melt temperature and lower t_o, is within the stability limit, but Case III (lower melt temperature) is unstable.

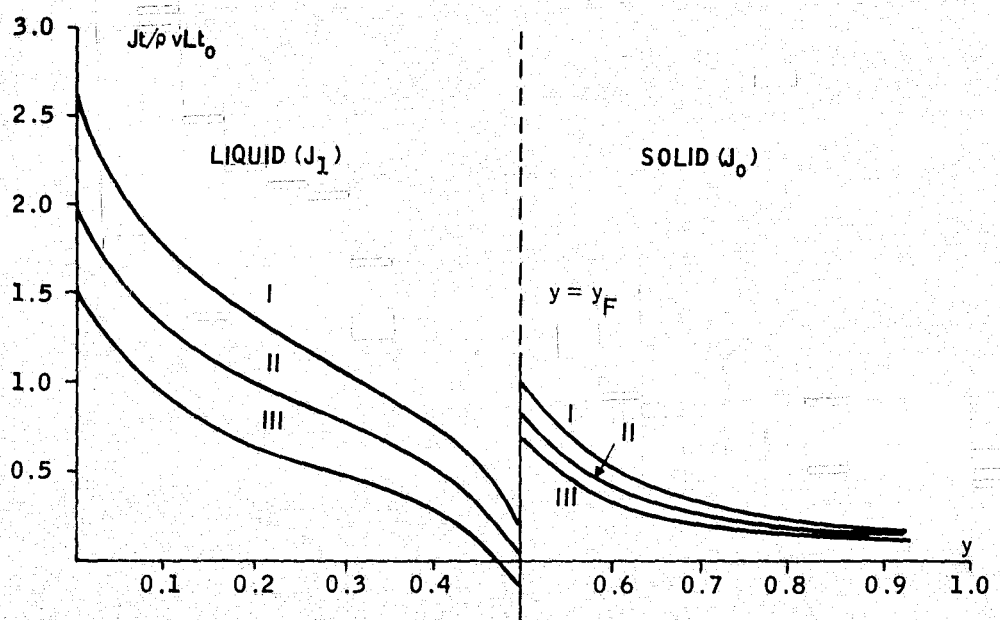


Figure 20. Normalized Thermal Flux in Liquid and Solid Parts of the Silicon Layer at Height y Above Melt Surface. v = 0.098 cm/sec for all three cases. The degree of stability is determined by the melt temperature. Case I (stable): $T_M - T_F = 22.3$ deg, $t_o = 0.0067$ cm, $J_1(y_F) > 0$. Case II (stable): $T_M - T_F = 15.1$ deg, $t_o = 0.0100$ cm, $J_1(y_F) = 0$. Case III (unstable): $T_M - T_F = 6.5$ deg, $t_o = 0.0143$ cm, $J_1(y_F) < 0$.

Figure 21 gives further computed data assuming the same fixed v. $J_1(y_F)$ is seen to be a monotonic increasing function of T_M, and t_o is a monotonic decreasing function of T_M. According to this figure, silicon thicknesses up to 0.01 cm can be stably grown at v = 0.098 cm/sec on 0.1-cm ceramic, assuming that heat is removed by radiation to an environment at room temperature.

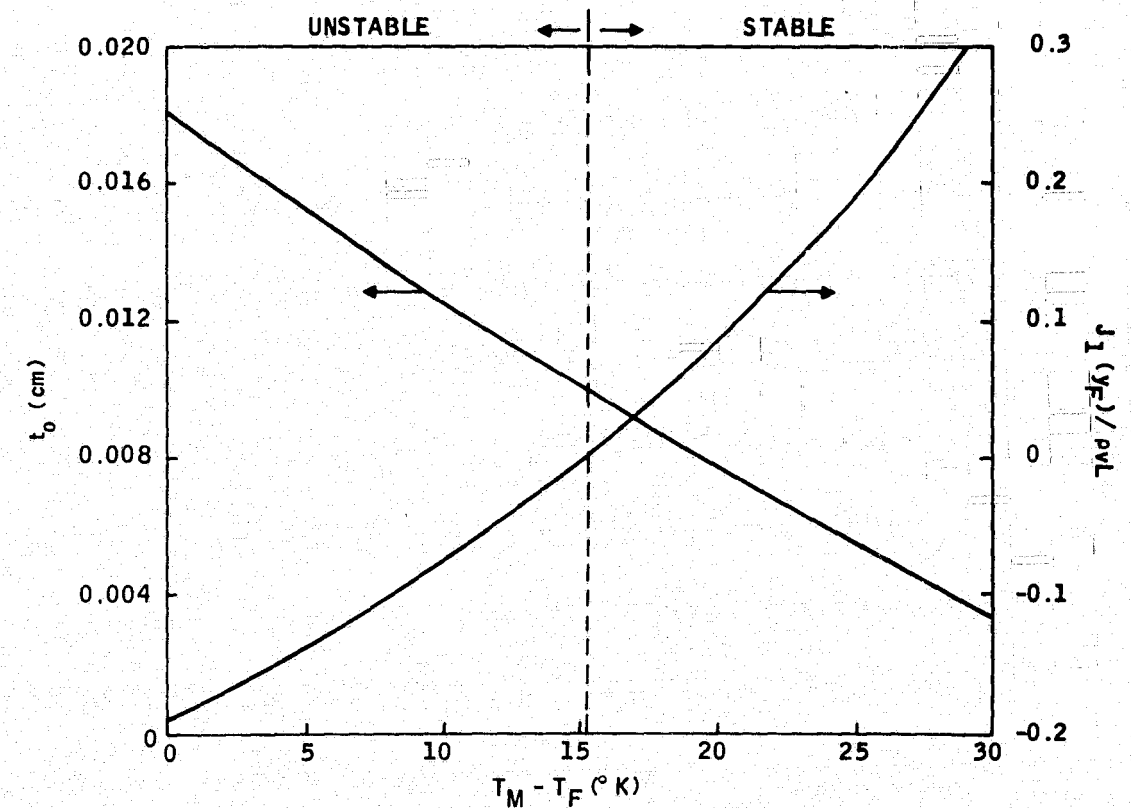


Figure 21. Normalized $J_1(y_F)$ and Silicon Thickness as Functions of Melt Temperature. Pull speed fixed at 0.098 cm/sec; t_c = 0.1 cm; $T_M - T_o$ = 1385°K; $T_M - T_1$ = 50°K; y_F = 0.5 cm.

Figure 22 shows t_o and $J_1(y_F)/\rho_o vL$ as functions of pull speed when melt temperature is held constant. We note that t_o always decreases as v increases, but $J_1(y_F)/\rho_o vL$ reaches a minimum and then increases with v. In general, the model indicates that growth is more stable at both extremes of pull speed (fixed T_M) and tends to become less stable or unstable at intermediate pull speeds. If a lower T_M were used in these calculations, there would be a larger range of pull speeds corresponding to unstable growth, and stable growth would be possible at both higher and lower pull speeds outside of this range.

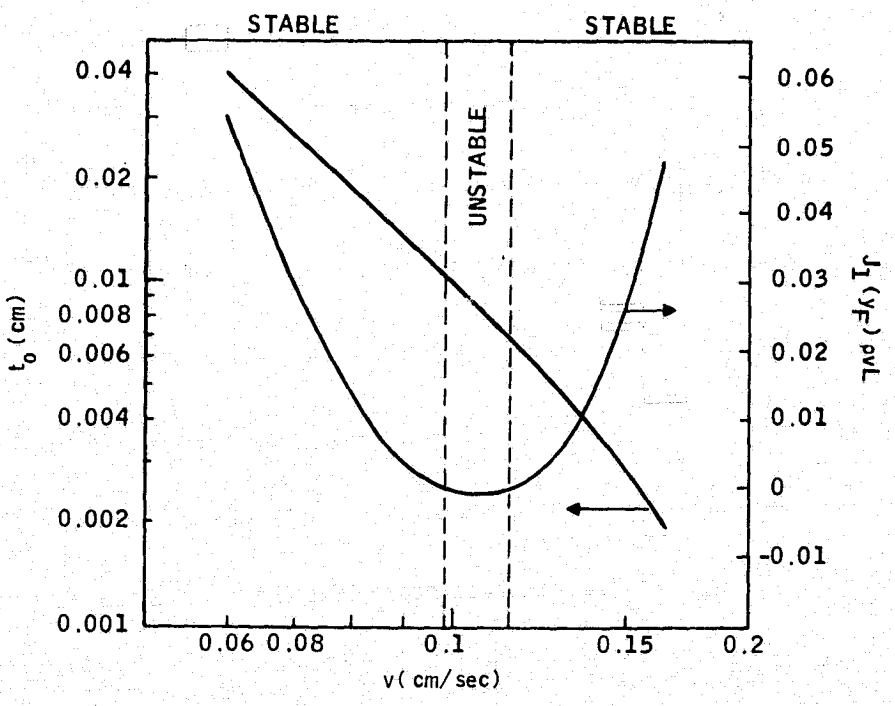


Figure 22. Normalized $J_1(y_F)$ and Silicon Thickness as Functions of Pull Speed. $T_M - T_F$ fixed at 15.1 deg; t_c = 0.1 cm; $T_M - T_o$ = 1385°K; $T_M - T_1$ = 50°K; y_F = 0.5 cm.

Figures 23a and 23b give conditions of limiting stable growth; in other words, v and T_M are simultaneously varied to keep $J_1(y_F) = 0$. The solid curves of Figure 23a compare the effects of high and low background temperature as well as two different substrate thicknesses. Dashed lines are limiting growth conditions for unsupported silicon from the one-dimensional analysis.[13] That analysis predicts a constant $v^2 t_o$ for each background temperature, giving straight lines with a slope of -2 on the logarithmic plot. On the other hand, the $v^2 t_o$ product for SOC is seen to fall rapidly at higher pull speeds, as thermal convection in the ceramic begins to dominate the heat disposal problem. The corresponding melt temperatures in Figure 23b all have maxima at intermediate pull speeds. This phenomenon, which is not readily explained, is consistent with the observations made in connection with Figure 22. The experimental data shown in Figure 23a were obtained with the "fast dipper" on 0.1-cm-thick ceramic with an undetermined background temperature.

The Role of T_1 and y_F

The calculations discussed so far have been based on the values y_F = 0.5 cm and $T_M - T_1$ = 50 degrees. To test the generality of the results, the calculations for the Figure 23a curves were repeated for two different combinations of y_F and T_1 : a) y_F = 0.69 cm, $T_1 - T_M$ = 50 degrees; b) y_F = 0.5 cm, $T_1 - T_M$ = 300 degrees. It was found that these

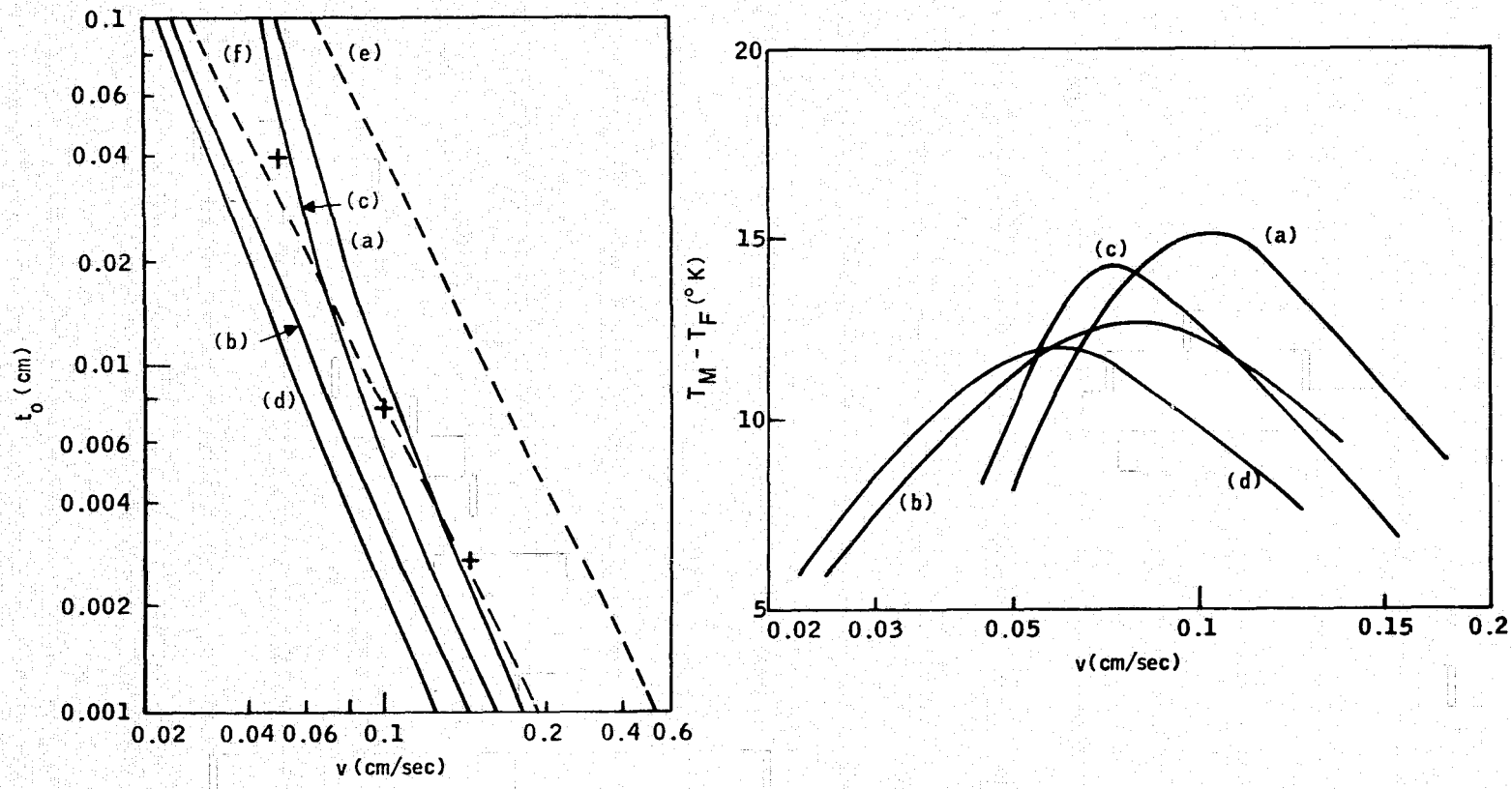


Figure 23. Silicon Thickness and Melt Temperature as Functions of Pull Speed for $J_1(y_F) = 0$ [limiting stable growth]. (a) $T_M - T_o = 1385°K$, $t_c = 0.1$ cm. (b) $T_M - T_o = 300°K$, $t_c = 0.1$ cm. (c) $T_M - T_o = 1385°K$, $t_c = 0.2$ cm. (d) $T_M - T_o = 300°K$, $t_c = 0.2$ cm. (e) $T_M - T_o = 1385°K$, $t_c = 0$ [unsupported growth]. (f) $T_M - T_o = 300°K$, $t_c = 0$. Experimental data (+) were obtained with the "fast dipper" on 0.1-cm ceramic.

new combinations gave the same limiting v versus t_o relationships as before. This is a surprising result and it indicates that neither of these parameters has a significant effect on the important limiting relationship. This also tends to support our earlier analysis of the unsupported sheet silicon growth, in which J_1 was assumed equal to zero, and further details of the liquid meniscus such as its shape and temperature distribution, were ignored.

Isotherm Shapes Within the Solid Silicon

The isotherms were assumed flat in the silicon part of the structure. The error in this assumption may be estimated by analyzing heat flows up the silicon and laterally toward the radiation and ceramic surfaces. In the solid silicon portion, the greatest departure from flatness occurs near the freezing isotherm itself, so the discussion is restricted to that region. No attempt is made to examine the liquid portion. We proceed as follows.

Let $\vec{j}_1$ and $\vec{j}_2$ be flux density vectors at the corners as shown in Figure 24. In a column of cross-section dxdz, the latent heat released per unit time is $\rho_o vLdxdz$. This is obviously the same quantity as $|\vec{j}_1|$ dsdz; hence,

$$|\vec{j}_1| = \rho_o vLdx/ds = \rho_o vL \cos \alpha_1 \tag{24}$$

Similarly,

$$|\vec{j}_2| = \rho_o vL \cos \alpha_2 \tag{25}$$

The lateral components are then

$$j_{1x} = \rho_o vL \sin \alpha_1 \cos \alpha_1 \tag{26}$$

$$j_{2x} = \rho_o vL \sin \alpha_2 \cos \alpha_2 \tag{27}$$

By continuity of lateral heat flow, j_{1x} is also the heat conducted into the ceramic:

$$j_{1x} = k_c \left|\partial T/\partial x\right| \tag{28}$$

and j_{2x} is the radiated heat

$$j_{2x} = \varepsilon_o \sigma \left(T_F^4 - T_o^4\right) \tag{29}$$

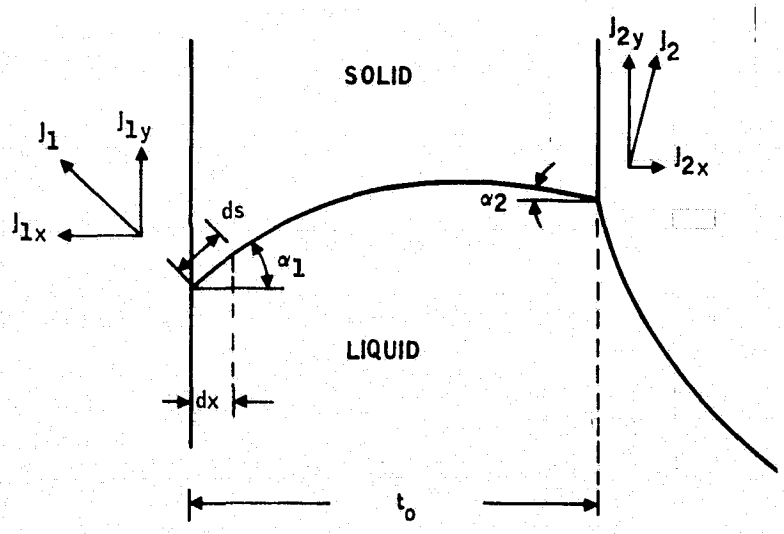


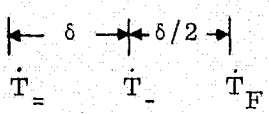
Figure 24. Analysis of Freezing Point Shape by Means of Heat Flux Components

Combining (26) with (28) and (27) with (29) gives

$$\alpha_1 = 1/2 \sin^{-1} \left\{ 2k_c \left| \partial T/\partial x \right| / \rho_o v L \right\} \tag{30}$$

$$\alpha_2 = 1/2 \sin^{-1} \left\{ 2\epsilon_o \sigma \left(T_F^4 - T_o^4 \right) / \rho_o v L \right\} \tag{31}$$

The angle α_2 may be evaluated directly, but for α_1 it is necessary to calculate $|\partial T/\partial x|$. A three-point interpolation formula may be used incorporating the calculated temperatures at $y = y_F$ and the last three columns in the finite difference lattice, recalling the spacing as shown:



The interpolation formula yields

$$\frac{\partial T}{\partial X} = \frac{1}{\delta} \left(\frac{8}{3} T_F - 3T_- + \frac{1}{3} T_= \right)$$

at the right-hand edge.

The angles α_1 and α_2 are plotted against thickness t_o in Figure 25 from data for the cold background case represented by the right-hand solid curve in Figure 23a. The maximum angles occur at the largest t_o, which is 0.1 cm. We restrict our attention to this con-

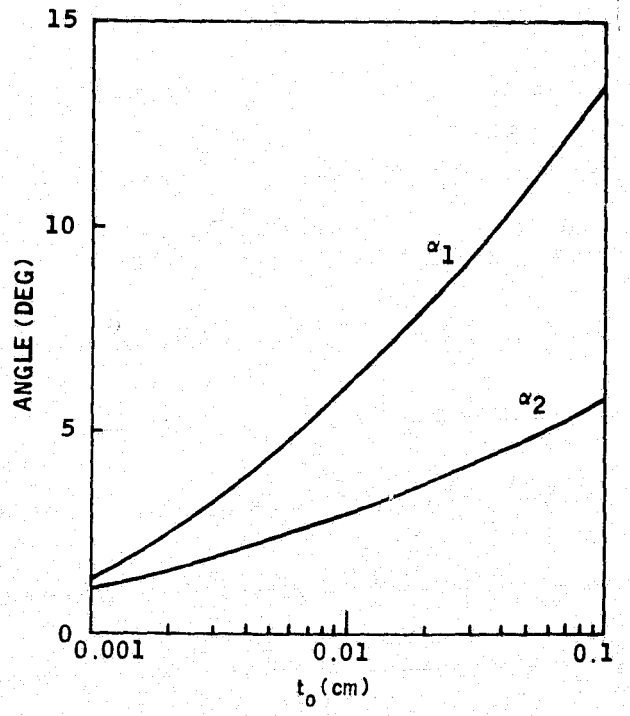


Figure 25. Inclinations of Freezing Isotherm versus Silicon Thickness. Growth conditions as in (a) of Figure 23. α_1 = inclination at silicon interface; α_2 = inclination at as-grown surface.

dition, which is the severest test of our flatness assumption. In Figure 26, that particular crytallization front is represented as a circular arc. From this geometry, the highest Δy spanned by the crystallization front is calculated to be 0.008 cm. Since the finite difference increment, δ, is 0.02 cm, we conclude that the worst-case Δy is only about half the numerical lattice spacing, and this justifies the flatness assumption.

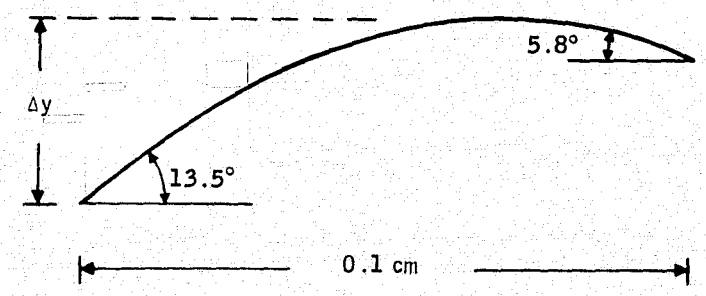


Figure 26. Approximate Worst-Case Crystallization Front Geometry (Exaggerated Scale)

It would be incorrect to conclude that most of the heat from the silicon is conducted into the substrate, although this is locally true near the interface, where $\alpha_1 > \alpha_2$. In fact, the angle α_1 decreases and eventually becomes negative with increasing height above the interface. In the net, heat flows from the ceramic into the silicon and not the other way around. This is certainly to be expected in view of the large contribution made by the substrate to the total heat that must be radiated away.

Summary

A steady-state vertical growth model for SOC yields a system of nonlinear, coupled differential equations for the temperature profiles in ceramic and silicon portions of the structure. Cooling of the structure is assumed to be by radiation to a specified environment, and the cooling rate must balance the rates of latent heat of fusion and convected heat from the melt. Liquid meniscus height is fixed by hydrostatic considerations and does not vary over the normal range of growth speed. Because of the complicated geometry and essential nonlinearity of the system, numerical solution of the equations is the method of choice.

Due to the overall heat balance requirement, only certain combinations of ceramic thickness (t_c), silicon coating thickness (t_o), pull speed (v), and melt temperature (T_M) will yield steady-state temperature profiles. In actual growth, the coating thickness is not arbitrarily specified but is a dependent function of t_c, v, and T_M ($>T_F$).

A theoretical stability criterion[17] places a further restriction on the allowable combinations of growth parameters. Growth is not stable if heat flows backwards from the crystallization fronts; in other words, stability requires that $d/dy\ U_1\ (y_F) \leq 0$. For a given pull speed, t_o increases monotonically as T_M is lowered toward T_F, but $d/dy\ U_1\ (y_F)$ increases (becomes less negative) at the same time. Maximum coating thickness for stable growth occurs therefore when $d/dy\ U_1\ (y_F) = 0$. This limiting thickness and the corresponding melt temperature both depend on pull speed, ceramic thickness, and radiation environment.

The limiting t_o versus v relationship has an economic significance in terms of process throughput and was investigated (Figure 23a) for various combinations of t_c and T_o. This was compared with unsupported silicon growth ($t_c = 0$). As expected, throughput is penalized by the presence of the substrate, especially at high pull speeds, due to the extra (sensible) heat input to the system.

Finally, the one-dimensional approximation in the solid-silicon portion was critically examined by estimating the maximum departure, Δy, from flatness for the freezing isotherm. This turned out to be of the order of 0.01 cm, which would appear to justify the approximation. Also, the freezing isotherm was found to be bowed upward, making a larger inclination to the horizontal at the ceramic surface than at the as-grown surface. Although most of the latent heat is carried vertically, this would indicate that the net lateral heat transfer in the neighborhood of the freezing front is into the ceramic as opposed to out from the free surface. This is true only locally, however. In fact, over the structure as a whole, net heat transfer across the silicon - ceramic interface is from ceramic to silicon.

CONCLUSIONS

From work performed during the quarter, we conclude that:

- Mullite substrates in a slotted configuration must contain excess silica to avoid breaking after dipping.
- Dye-checking the slotted substrates for cracks increases the yield of coated substrates.
- Hand-rubbed carbon coatings are applied to slotted substrates instead of colloidal graphite so as to avoid silicon entering the slots during dipping.
- The silica content of the mullite substrate must be high enough to obtain a good thermal expansion match with silicon but not so high as to make the substrate "soft" at the melting temperature of silicon.
- The relationship between coating velocity and thickness for dip-coating SOC material follows a v^2t = constant, relationship. The value of this constant increases as external cooling is added to the coating process.
- Continuous coating of substrates can be obtained using our SCIM coating facility. Tight control of the thermal gradients near the solidification zone is necessary to produce large-area coatings.
- The absolute value of our SOC/single-crystal solar cell conversion efficiency is not known. Using a standard reference cell obtained from JPL yields best SOC results of 9.6 percent coated total-area conversion efficiency.
- We have a standard process for fabricating slotted SOC solar cells which yields reproducible results.
- The parameter which offers the greatest room for improvement in overall performance is J_{sc}.

- Recent results indicate the integral optical coupler (IOC) concept is viable. Further work must be done to improve fabrication techniques in order to provide higher overall performance.
- Back Surface Field (BSF) studies on SOC material have shown negative results to date.
- Recent observations indicate that the angle of the liquid - solid interface tilts away from the substrate - silicon interface in the neighborhood of the freezing front.
- An analytical analysis of our dip-coating process indicates that our ceramic substrate may penalize us thermally at high pull speeds.

RECOMMENDATIONS

To date, we have carried on an effort in an attempt to provide a Back Surface Field (BSF) effect in our SOC material using various aluminum pastes. This activity has not proven successful. We recommend a cessation of this activity and more emphasis placed on improvement of slotted-cell processing techniques.

PROJECTION OF FUTURE ACTIVITIES

Future activities are projected as follows:

- Characterization of the mechanical properties of the latest new mullite compositions for slotted substrates will continue.
- Both dip coaters will be dedicated initially to providing material for JPL disbursement to outside contractors for cell fabrication.
- The production dip coater will be used to provide cell material and evaluate new-composition slotted substrates.
- The experimental dip coater will be used to increase the speed - thickness product by further investigating external cooling near the solidification front.
- The thermal gradients at the solidification area in the SCIM coater will be modified to provide for larger-area continuous coatings. Elevation of the downstream end of the coater may be used to improve coating performance.
- Material evaluation will be carried out in an attempt to understand what is limiting the J_{sc} parameter of our SOC material.
- Efforts will be undertaken to systematically improve our SOC slotted-cell processing techniques.
- The "2X" IOC cell activity will be continued, with increased emphasis on the improvement of SOC stripe-cell processing techniques.
- Analytical work will continue in an attempt to understand the strengths and weaknesses of the supported growth concept using a ceramic substrate.

NEW TECHNOLOGY

There were no reportable "new technology" items uncovered during this reporting period.

Updated versions of the Program Plan, Program Labor Summary, and Program Cost Summary are presented in Figures 26, 27, and 28 respectively.

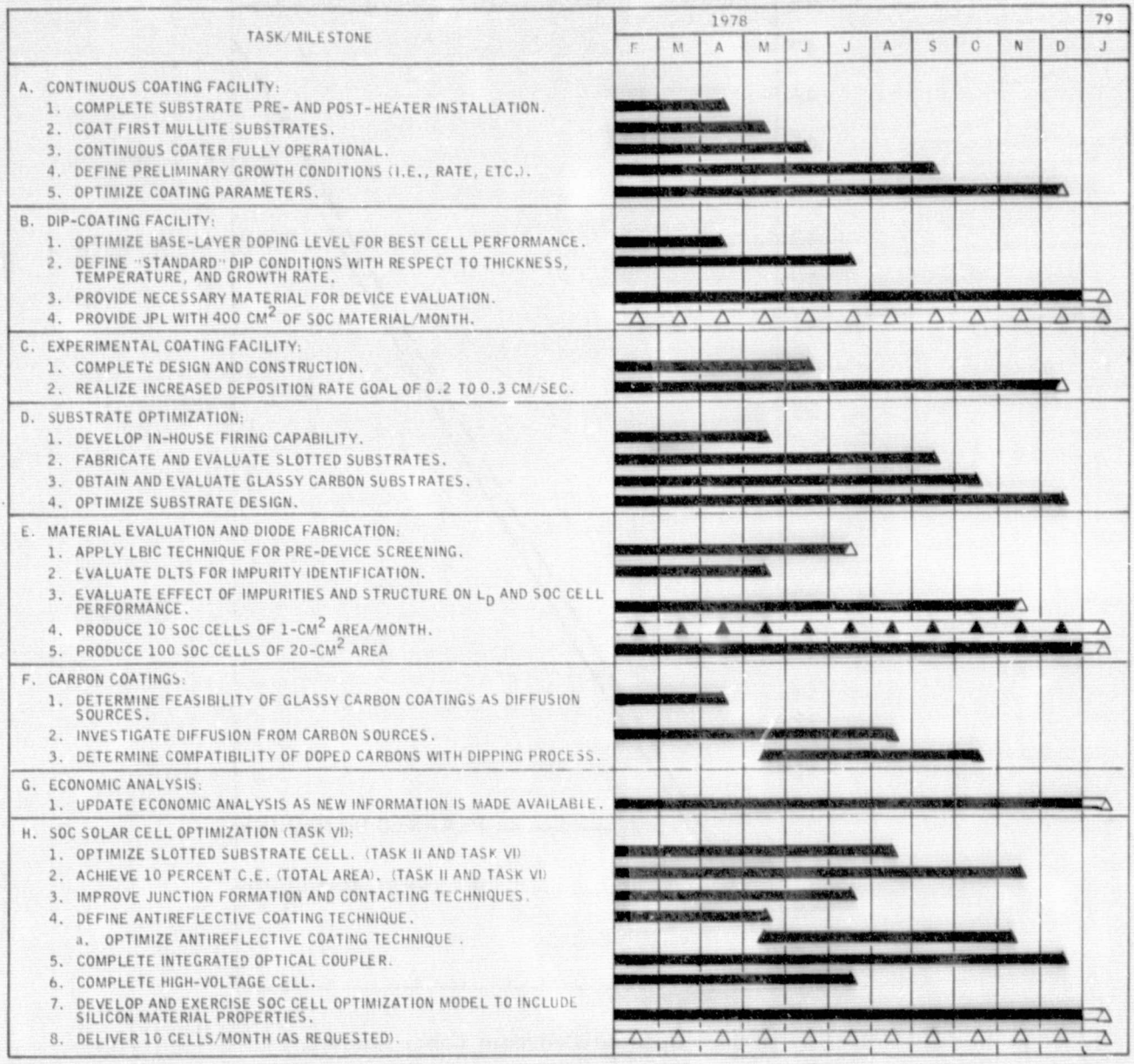


Figure 26. Updated Program Plan

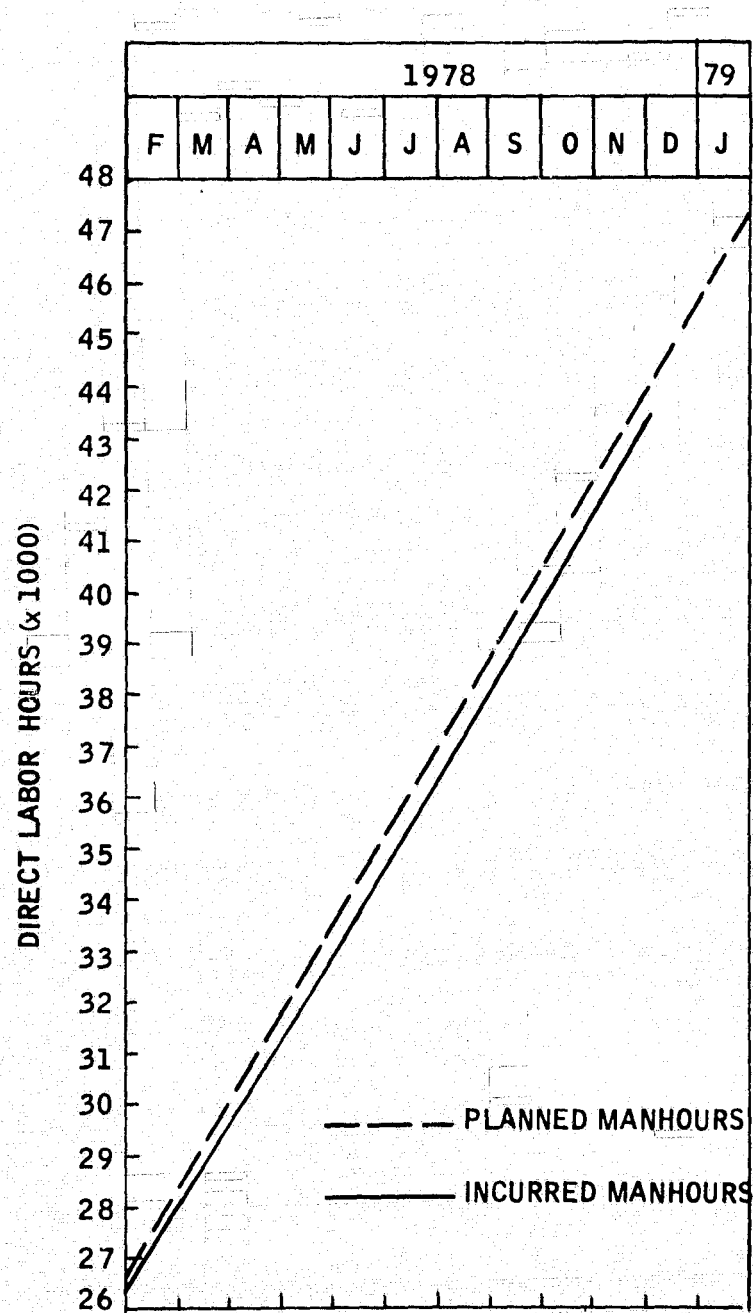


Figure 27. Updated Program Labor Summary

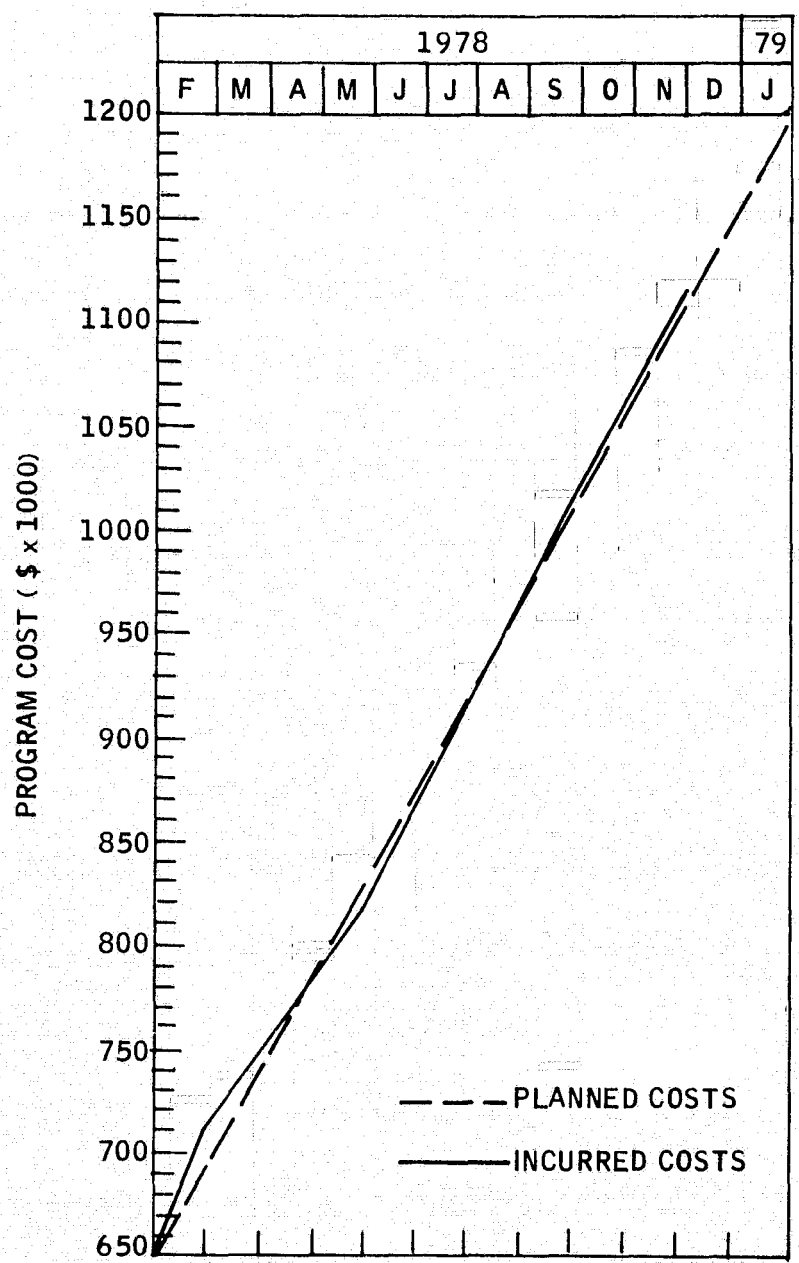


Figure 28. Updated Program Cost Summary

REFERENCES

1. D. G. Wirth and J. D. Sibold, Quarterly Report to JPL on Contract 954878, Coors Porcelain Co., Golden, CO, November 15 (1978).

2. J. D. Sibold, Coors Porcelain Co., Golden, CO, private communication (December, 1978).

3. "Relationship of contact angles to interfacial energies," J. E. McNutt and G. M. Audes, J. Chem. Phys. 30, 1300-1303 (1959).

4. "The direction of growth of the surface of a crystal in contact with its melt," T. Surek and B. Chalmers, J. Cryst. Growth 29, 1-11 (1975).

5. "The EFG process applied to growth of silicon ribbons," J. G. Suartz, T. Surek, and B. Chalmers, J. Electronic Materials 4, 255-279 (1975).

6. "Thermal analysis of single-crystal silicon ribbon growth processes," A. E. Bell, RCA Review 38, 109-139 (1977).

7. "Maximum growth rates for melt-grown-ribbon-shaped crystals," T. F. Ciszek, J. Appl. Phys. 47, 440-442 (1976).

8. "The edge-defined film-fed growth of controlled-shape crystals," T. Surek and S. R. Coriell, J. Cryst. Growth 37, 253-271 (1977).

9. "Surface morphology end shape stability in silicon ribbons grown by the edge-defined, film-fed process," T. Surek, C. B. Hari Rao, J. C. Swartz, and L. C. Garme, J. Electrochem. Soc., 124, 112-123 (1977).

10. "Thermal analysis of solidification in wet-dendritic ribbon growth," M. D. Harril, G. A. Rhodes, J. W. Faust, and R. B. Hilborn, J. Crystal Growth, 44, 34-44 (1978).

11. "Growth, evaluation, and modeling of silicon-on-ceramic solar cells," J. D. Zook, S. B. Schuldt, R. B. Maciolek, and J. D. Heaps, Thirteenth Photovoltaic Specialists Conference, 1978, IEEE Press (1978), pp. 972-978.

12. "Continuous polycrystalline silicon layers on carbon substrates," C. Belouet, J. J. Prissot, R. Wartres, Ngo Tich Phoc., in Photovoltaic Solar Energy Conference, Luxembourg, September 1977, D. Reidel Publishing, Holland (1978).

13. "Analysis of conditions for high-speed growth of silicon sheet," J. D. Zook and S. B. Schuldt, to be published.

14. "Supported growth of sheet silicon from the melt," R. B. Maciolek, B. G. Koepke, M. Leipold, and J. D. Zook, to be published.

15. Conduction of Heat in Solids, H. S. Carslaw and J. C. Jaeger, 2nd ed., Oxford University Press (1959).

16. Numerical Solution of Ordinary and Partial Differential Equations, L. Fox, Pergamon Press (1962), p. 289.

17. The Growth of Crystals from Liquids, J. C. Brice, North Holland Press (1973), pp. 160-170.

18. "Conductivity of the elements: a comprehensive review," C. Y. Ho, R. W. Powell, and P. E. Liley, J. Phys. Chem. Ref. Data, Vol. 3, Suppl. 1 (1974), p. I-588.